

HD74LS107A

Dual J-K Negative-edge-triggered Flip-Flops (with Clear)

REJ03D0425-0300

Rev.3.00

Jul.13.2005

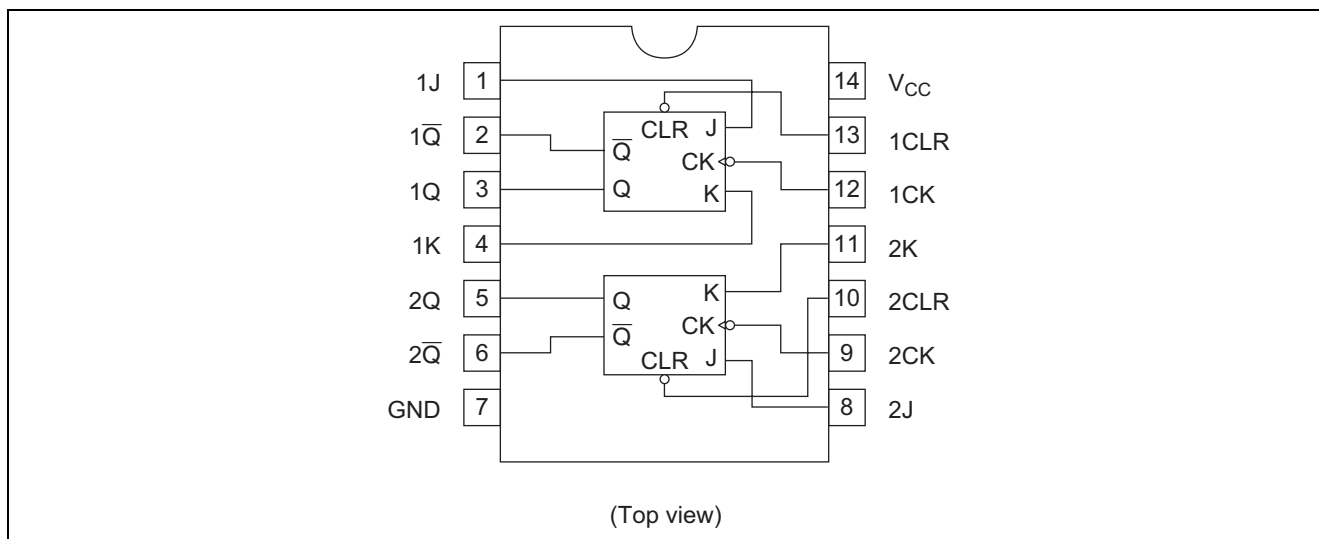
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS107AP	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—
HD74LS107AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

Inputs				Outputs	
Clear	Clock	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\bar{Q}_0$

Notes: H; high level, L; low level, X; irrelevant

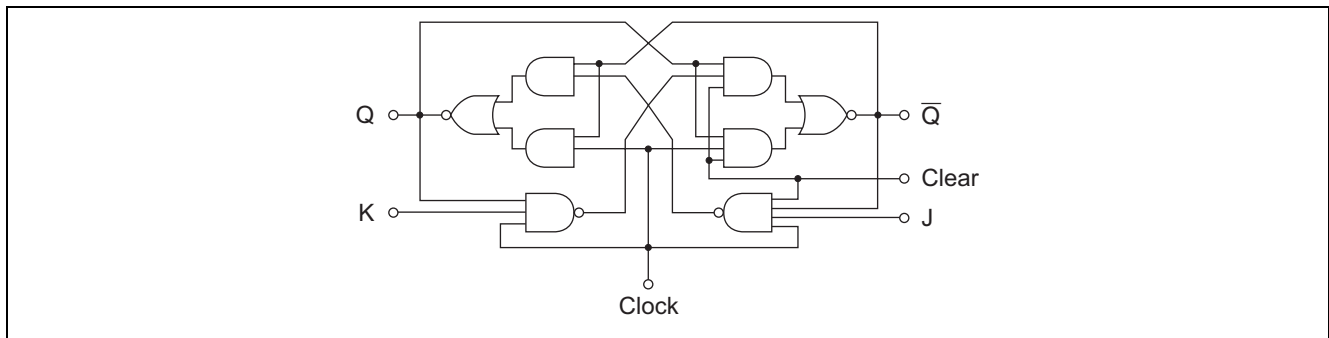
↓; transition from high to low level

Q_0 ; level of Q before the indicated steady-state input conditions were established.

$\bar{Q}_0$; complement of Q_0 or level of $\bar{Q}$ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	-400	μA
	I_{OL}	—	—	8	mA
Operating temperature	T_{opr}	-20	25	75	°C
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	t_w	20	—	ns
	Clear Low		25	—	ns
Setup time	"H" Data	t_{su}	20↓	—	ns
	"L" Data		20↓	—	ns
Hold time	t_h	0↓	—	—	ns

Electrical Characteristics

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition
Input voltage		V _{IH}	2.0	—	—	V	
		V _{IL}	—	—	0.8	V	
Output voltage		V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -400 μA
		V _{OL}	—	—	0.5	V	I _{OL} = 8 mA
			—	—	0.4		I _{OL} = 4 mA
Input current	J, K	I _{IH}	—	—	20	μA	V _{CC} = 5.25 V, V _I = 2.7 V
	Clear		—	—	60		
	Clock		—	—	80		
	J, K	I _{IL}	—	—	-0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V
	Clear		—	—	-0.8		
	Clock		—	—	-0.8		
	J, K	I _I	—	—	0.1	mA	V _{CC} = 5.25 V, V _I = 7 V
	Clear		—	—	0.3		
	Clock		—	—	0.4		
Short-circuit output current		I _{OS}	-20	—	-100	mA	V _{CC} = 5.25 V
Supply current**		I _{CC}	—	4	6	mA	V _{CC} = 5.25 V
Input clamp voltage		V _{IK}	—	—	-1.5	V	V _{CC} = 4.75 V, I _{IN} = -18 mA

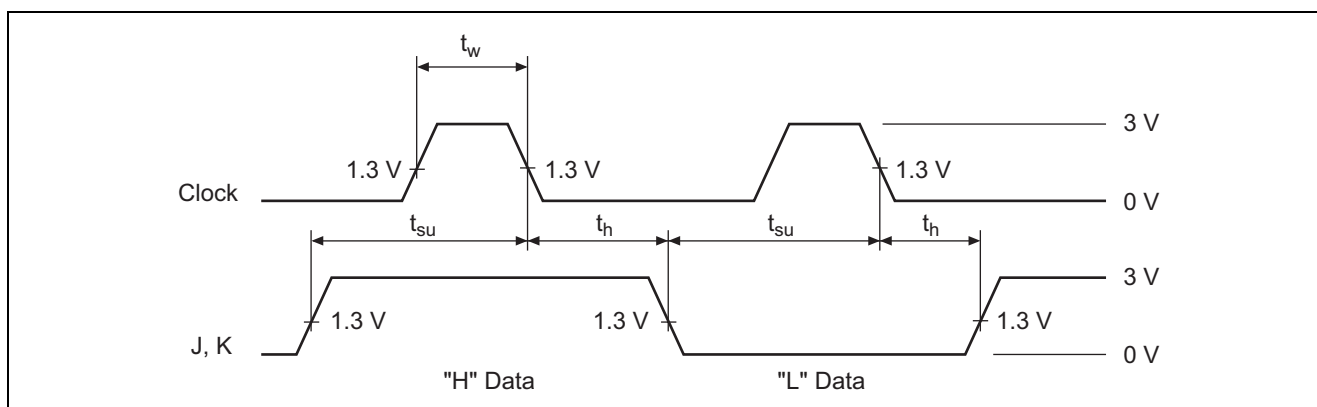
Notes: * V_{CC} = 5 V, Ta = 25°C** With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the times of measurement, the clock input is grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f _{max}			30	45	—	MHz	C _L = 15 pF, R _L = 2 kΩ
Propagation delay time	t _{PLH}	Clear	Q, $\bar{Q}$	—	15	20	ns	
	t _{PHL}	Clock		—	15	20	ns	

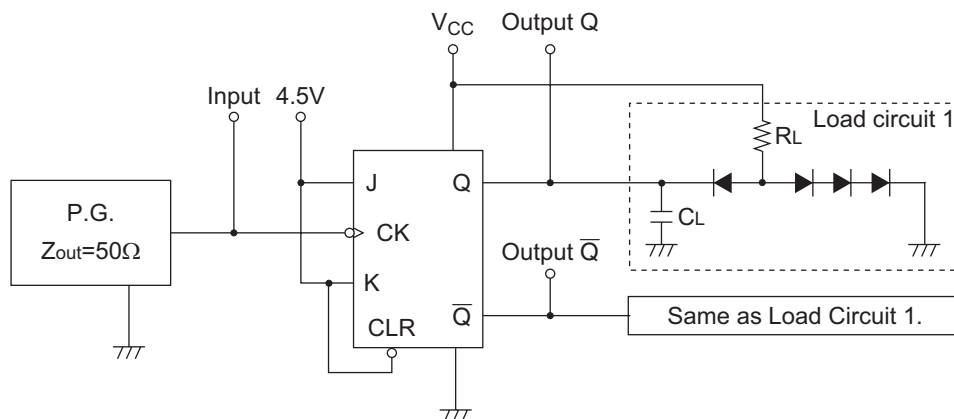
Timing Definition



Testing Method

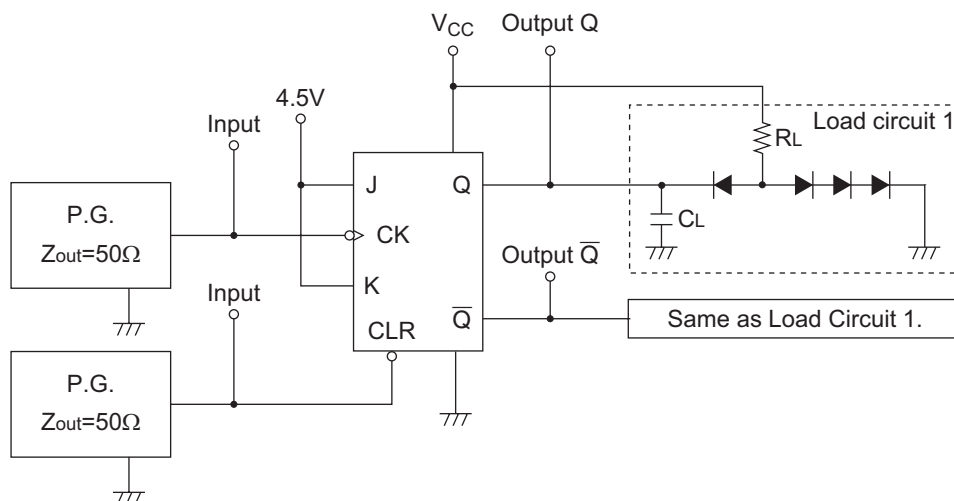
Test Circuit

1. $f_{\max}$, t_{PLH} , t_{PHL} , (Clock $\rightarrow$ Q, $\bar{Q}$)



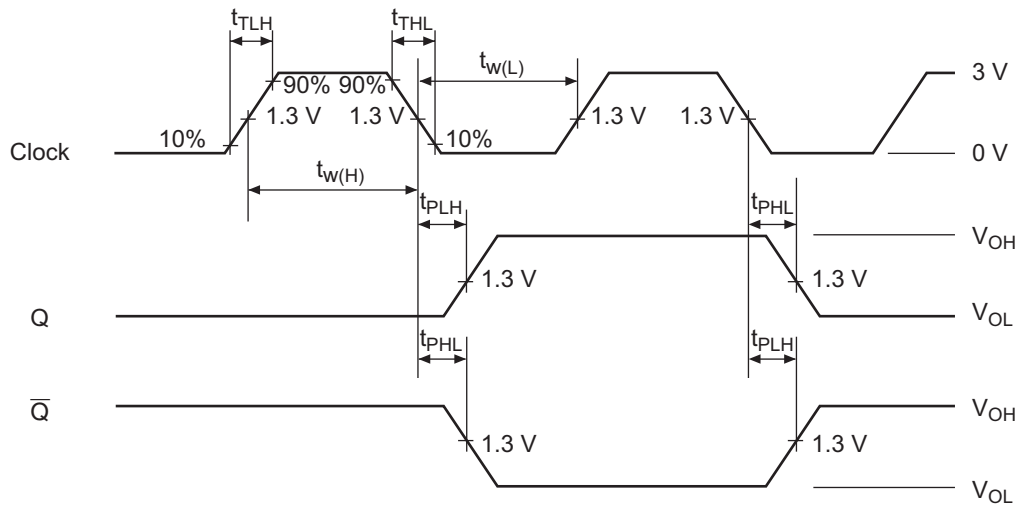
- Notes:
1. Test is put into the each flip-flop.
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074(H).

2. t_{PHL} (Clear $\rightarrow$ Q), t_{PLH} (Clear $\rightarrow$ $\bar{Q}$)



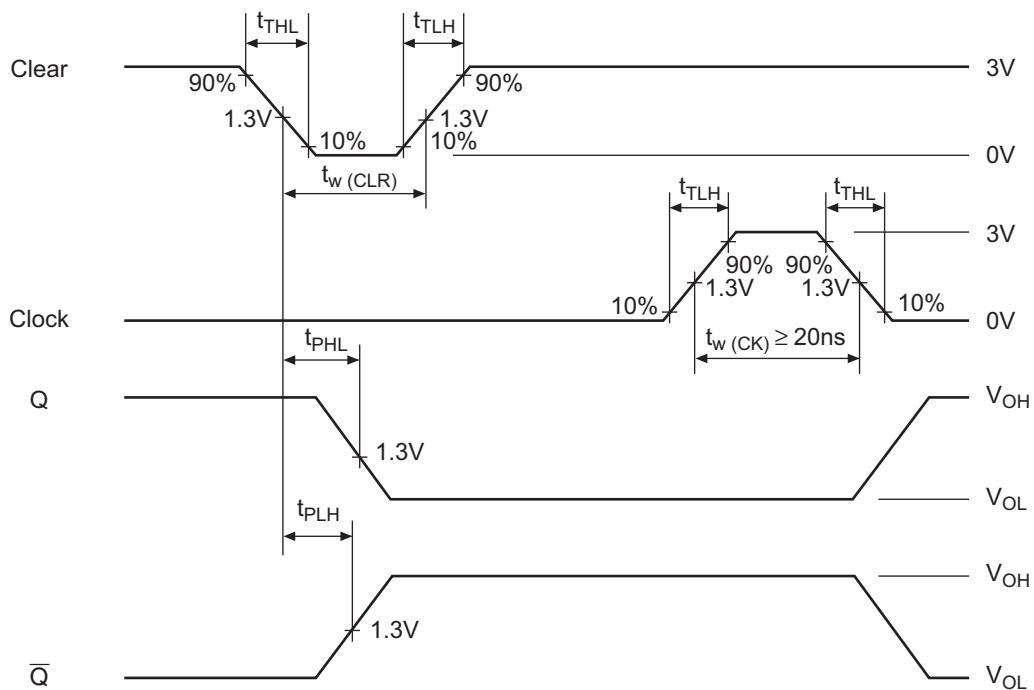
- Notes:
1. Test is put into the each flip-flop.
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Waveforms 1



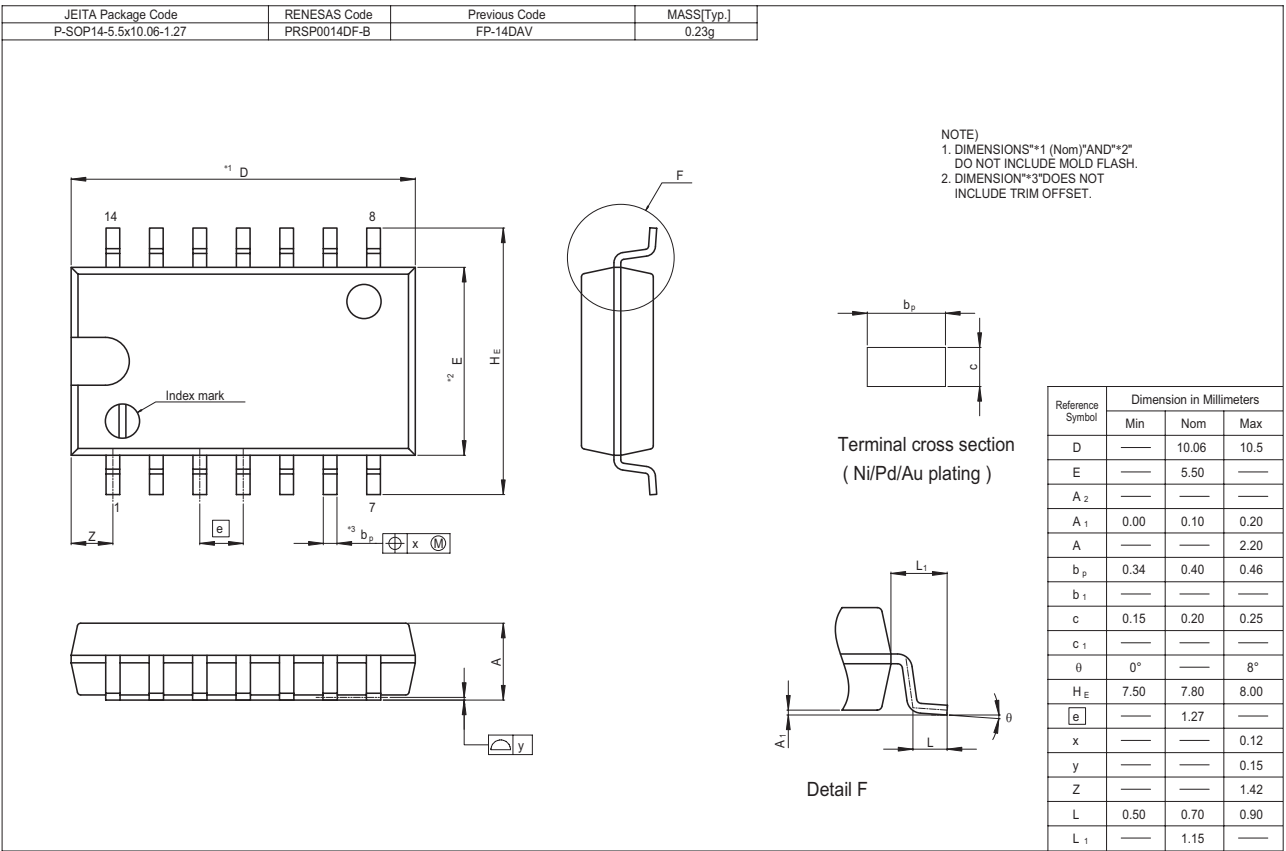
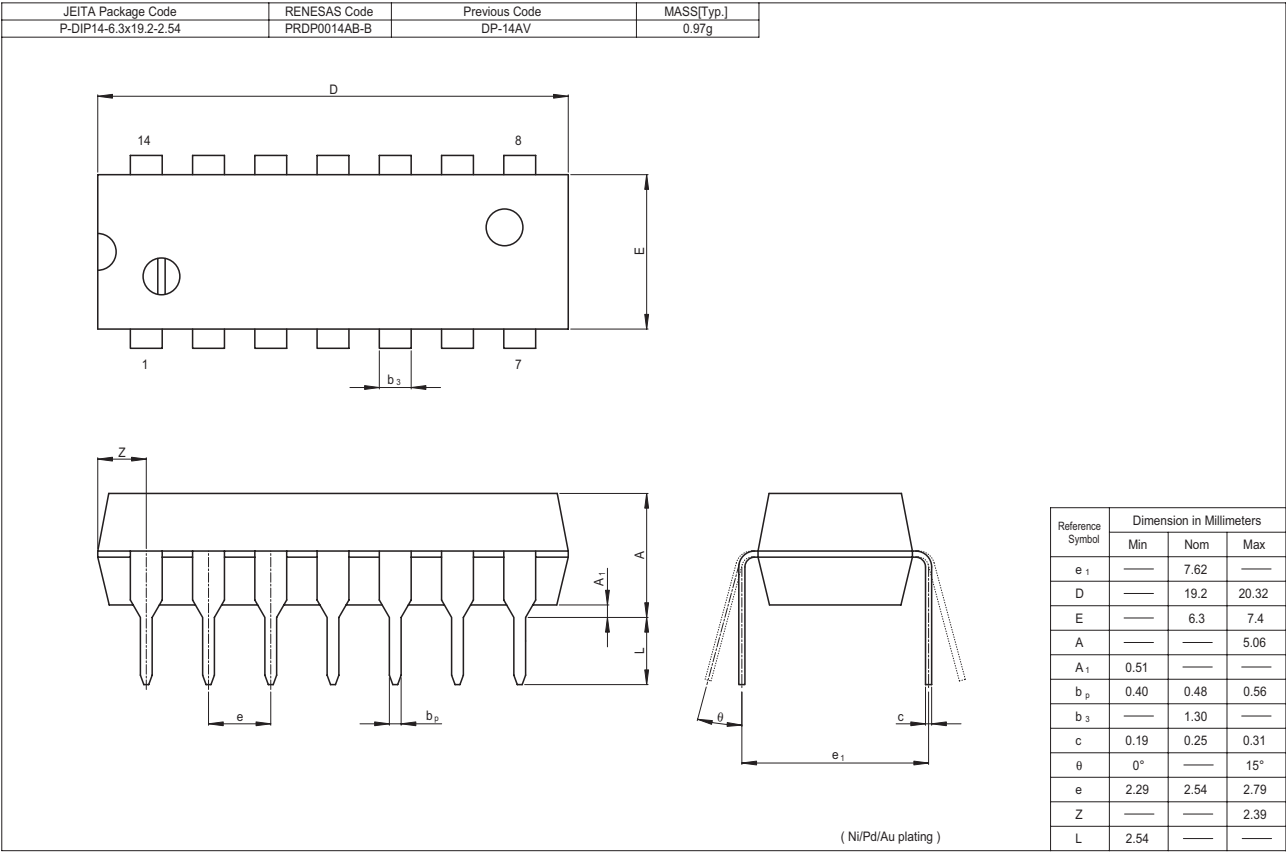
Note: Clock input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and: for f_{max} , t_{TLH} $t_{THL} \leq 2.5$ ns.

Waveforms 2



Note: Clear and clock input pulse: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz.

Package Dimensions



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