HD74LS293

4-bit Binary Counter

REJ03D0477–0300
Rev.3.00
Jul.15.2005

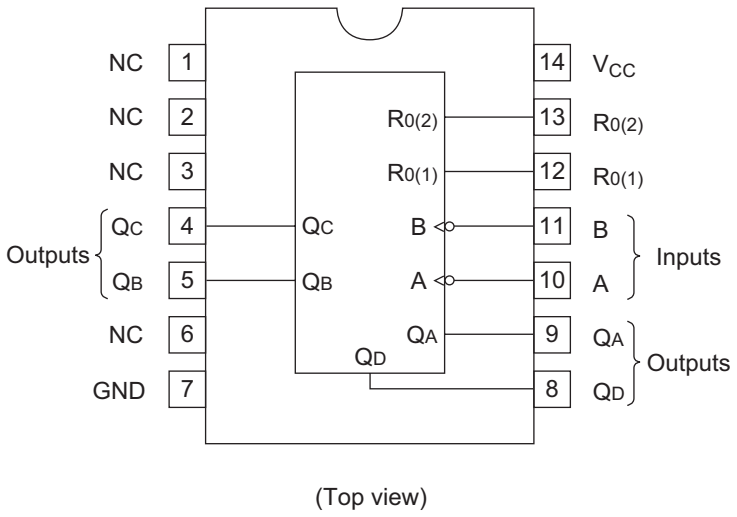
This counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and divide-by-eight counter. This counter has a gated zero reset. To use the maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS293P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—

Pin Arrangement



(Top view)

Function Table

Reset / Count

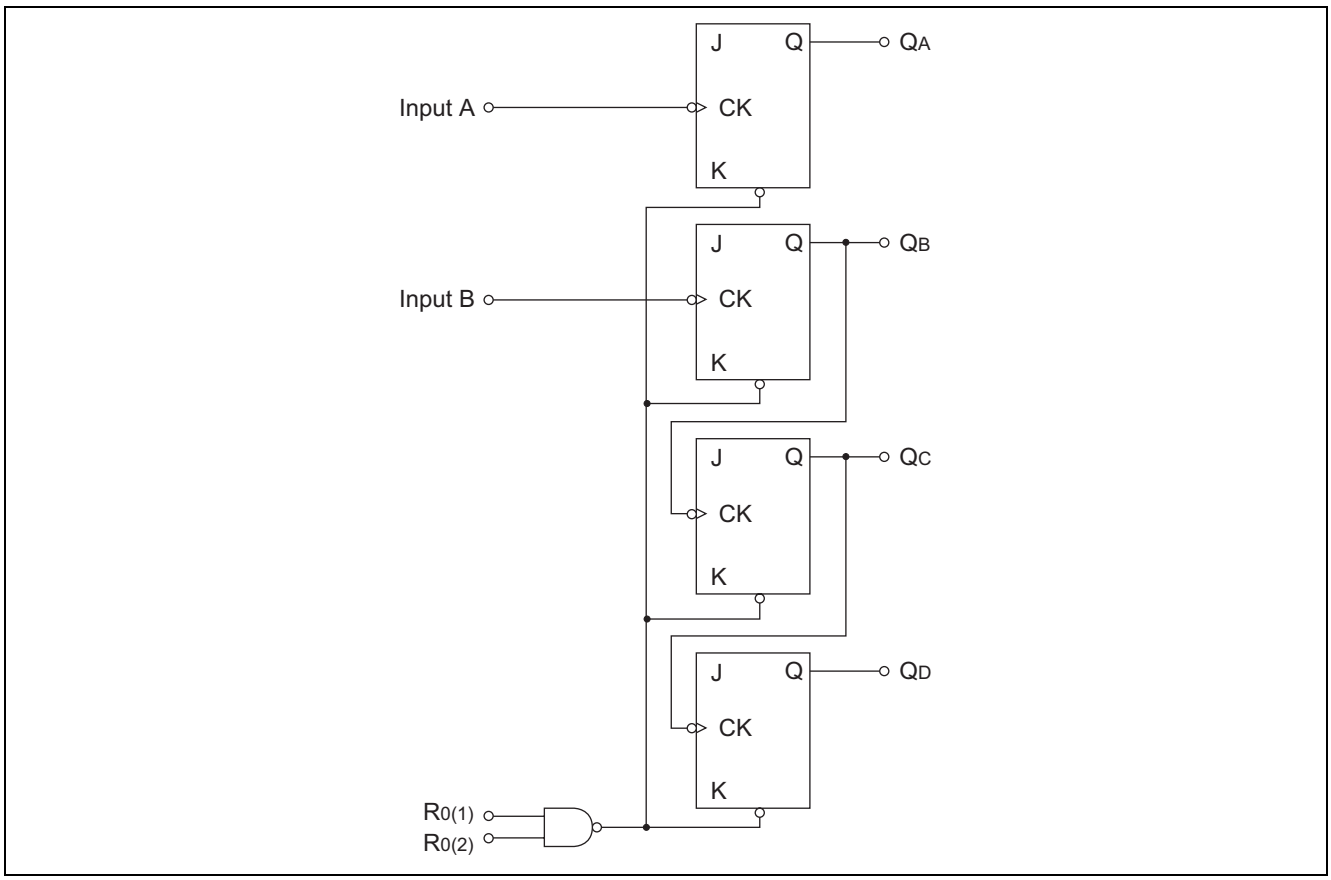
Reset Input		Outputs			
$R_{0\,(1)}$	$R_{0\,(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

BCD Count Sequence

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes: 1. H; high level, L; low level, X; irrelevant
2. Output Q_A is connected to input B.

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7	V
Input voltage	R_O Inputs	V_{IN}	7	V
	A, B Inputs		5.5	V
Power dissipation		P_T	400	mW
Operating temperature		Topr	–20 to +75	°C
Storage temperature		Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	–400	µA
		I_{OL}	—	—	8	mA
Operating temperature		Topr	–20	25	75	°C
Count frequency	A input	f_{count}	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	t_w	15	—	—	ns
	B input		30	—	—	
	Reset inputs		15	—	—	
Setup time		t_{su}	25	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V_{IH}	2.0	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA	
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA**	V_{CC} = 4.75 V,
			—	—	0.5		I_{OL} = 8 mA**	V_{IH} = 2 V, V_{IL} = 0.8 V
Input current	Any Reset	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	A input		—	—	40			
	B input		—	—	40			
	Any Reset	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	A input		—	—	–2.4			
	B input		—	—	–1.6			
	Any Reset	I_I	—	—	0.1	mA	V_I = 7 V	V_{CC} = 5.25 V
	A input		—	—	0.2		V_I = 5.5 V	
	B input		—	—	0.2			
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V	
Supply current***		I_{CC}	—	9	15	mA	V_{CC} = 5.25 V	
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Notes: * V_{CC} = 5 V, Ta = 25°C

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

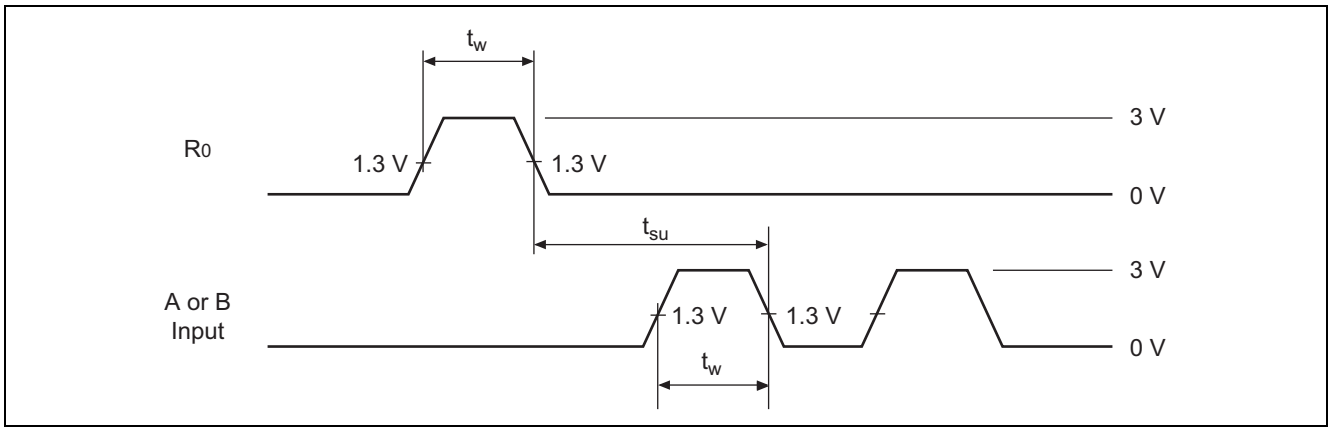
*** I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

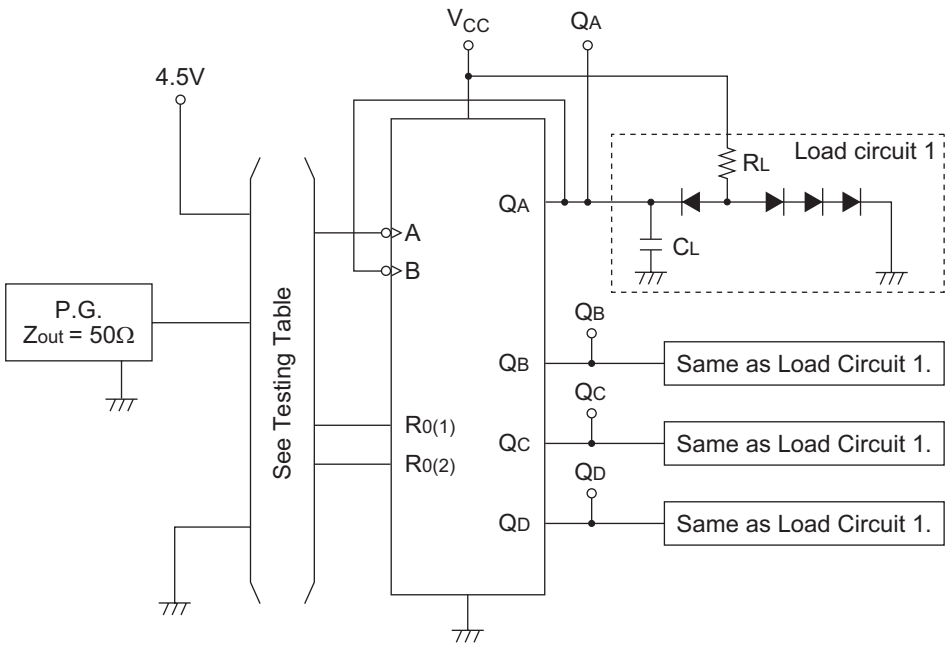
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	f_{max}	A	Q_A	32	42	—	MHz	C_L = 15 pF, R_L = 2 kΩ
		B	Q_B	16	—	—		
Propagation delay time	t_{PLH}	A	Q_A	—	10	16	ns	
	t_{PHL}			—	12	18		
	t_{PLH}	A	Q_D	—	46	70	ns	
	t_{PHL}			—	46	70		
	t_{PLH}	B	Q_B	—	10	16	ns	
	t_{PHL}			—	14	21		
	t_{PLH}	B	Q_C	—	21	32	ns	
	t_{PHL}			—	23	35		
	t_{PLH}	B	Q_D	—	34	51	ns	
	t_{PHL}			—	34	51		
	t_{PHL}	Set-to-0	Q_A to Q_D	—	26	40	ns	

Timing Method



Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

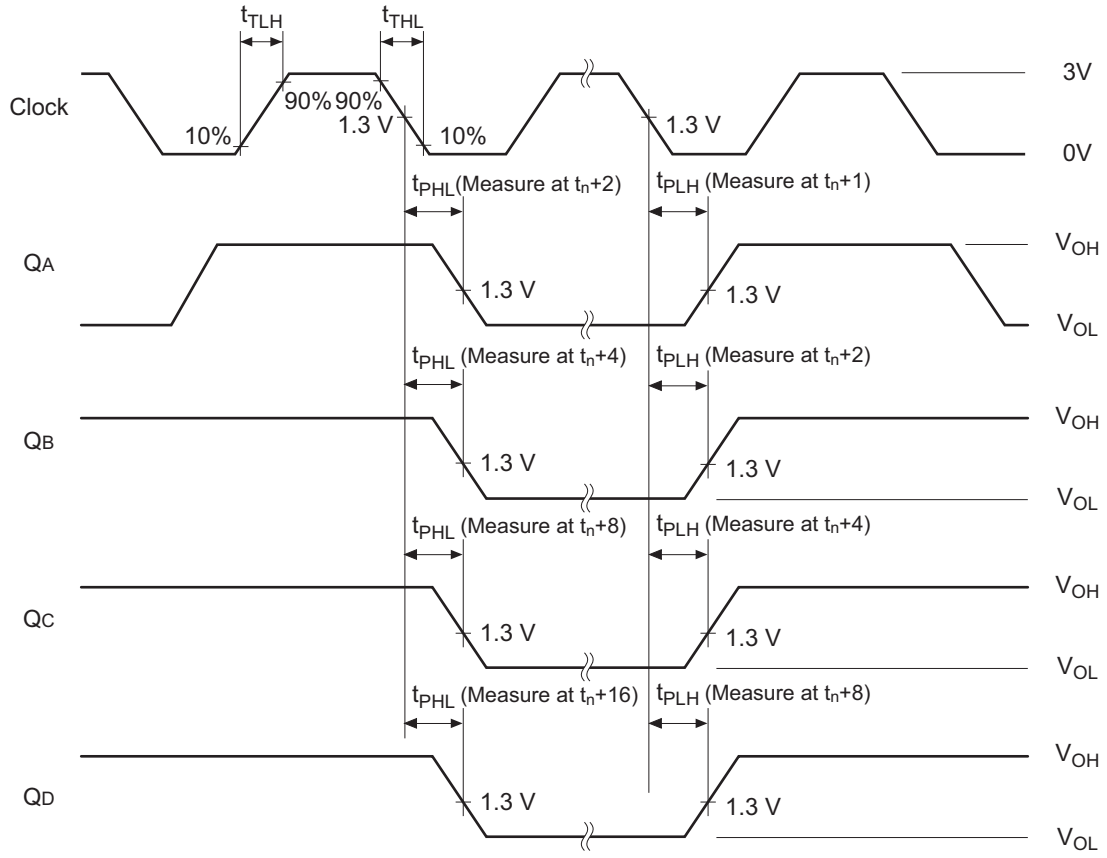
Testing Table

Item	From input to output	Inputs			Outputs			
		A	B	R_0	Q_A	Q_B	Q_C	Q_D
f_{max}	A→Q	IN	to Q_A	GND	OUT	OUT	OUT	OUT
	B→Q	4.5V	IN	GND	—	OUT	OUT	OUT
t_{PLH} t_{PHL}	A→Q_A	IN	to Q_A	GND	OUT	—	—	—
	A→Q_D	IN	to Q_A	GND	—	—	—	OUT
	B→Q_B	4.5V	IN	GND	—	OUT	—	—
	B→Q_C	4.5V	IN	GND	—	—	OUT	—
	B→Q_D	4.5V	IN	GND	—	—	—	OUT
	R_0→Q**	IN*	to Q_A	IN	OUT	OUT	OUT	OUT

Notes: * For initialized.
** Measured with each input and unused inputs at 4.5 V.

Waveforms 1

f_{max}, t_{PLH}, t_{PHL}, (Clock→Q)

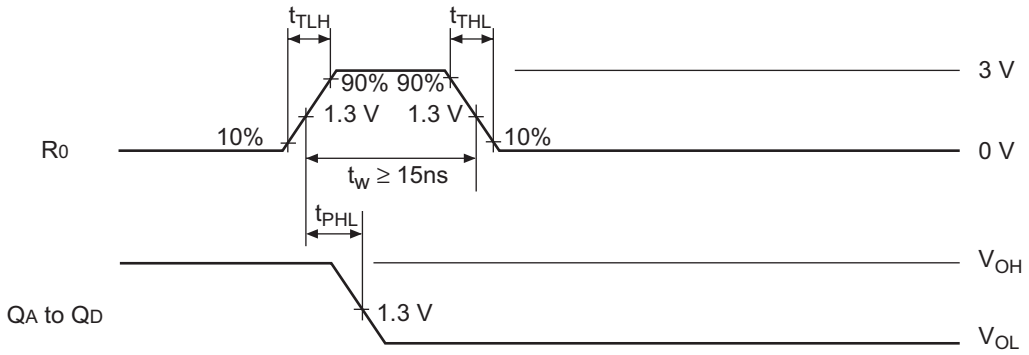


Notes: 1. Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and : for f_{max}, $t_{TLH} = t_{THL} \leq 2.5$ ns.

2. t_n is reference bit time when all outputs are low.

Waveforms 2

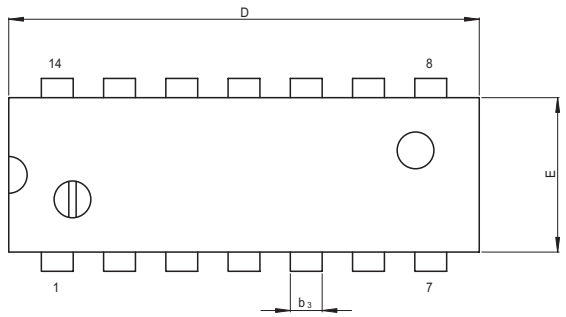
t_{PHL}, (R_0→Q)

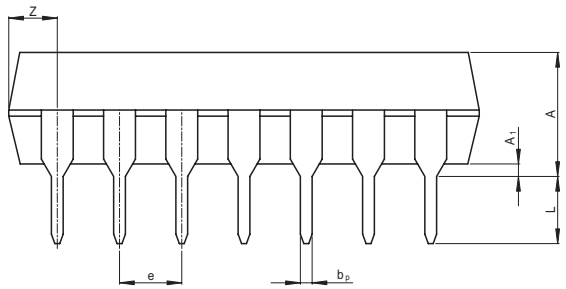


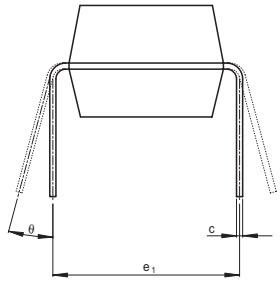
Note: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 5$ ns

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP14-6.3x19.2-2.54	PRDP0014AB-B	DP-14AV	0.97g







(Ni/Pd/Au plating)

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A_1	0.51	——	——
b_p	0.40	0.48	0.56
b_3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	2.39
L	2.54	——	——

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