

HD74LS293

4-bit Binary Counter

REJ03D0477-0300

Rev.3.00

Jul.15.2005

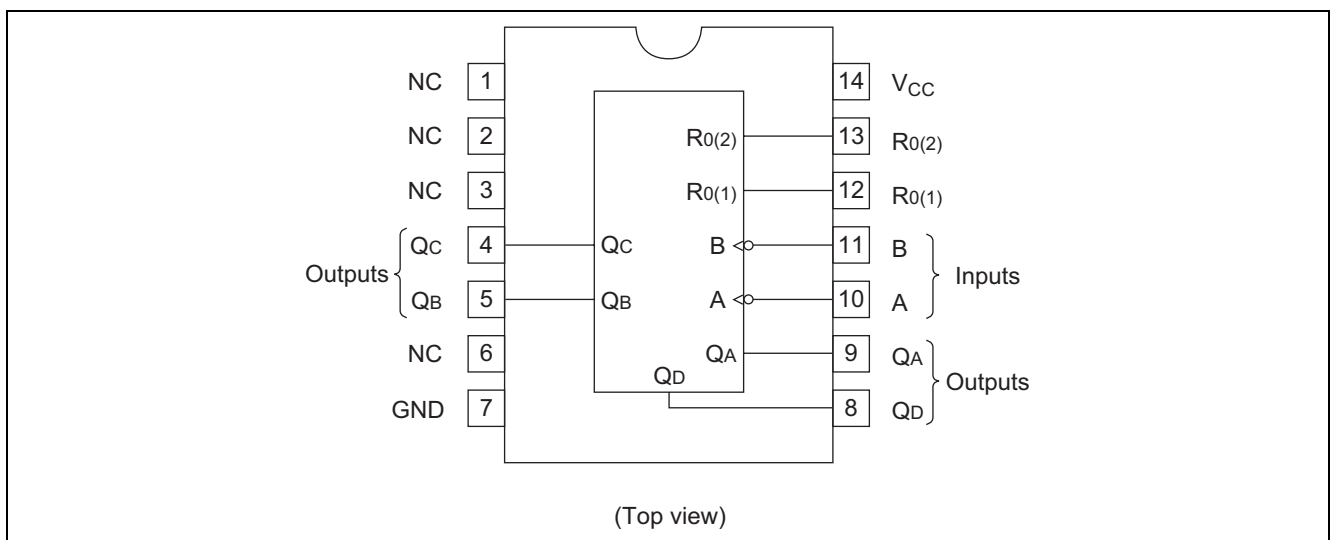
This counter contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and divide-by-eight counter. This counter has a gated zero reset. To use the maximum count length of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS293P	DILP-14 pin	PRDP0014AB-B (DP-14AV)	P	—

Pin Arrangement



Function Table

Reset / Count

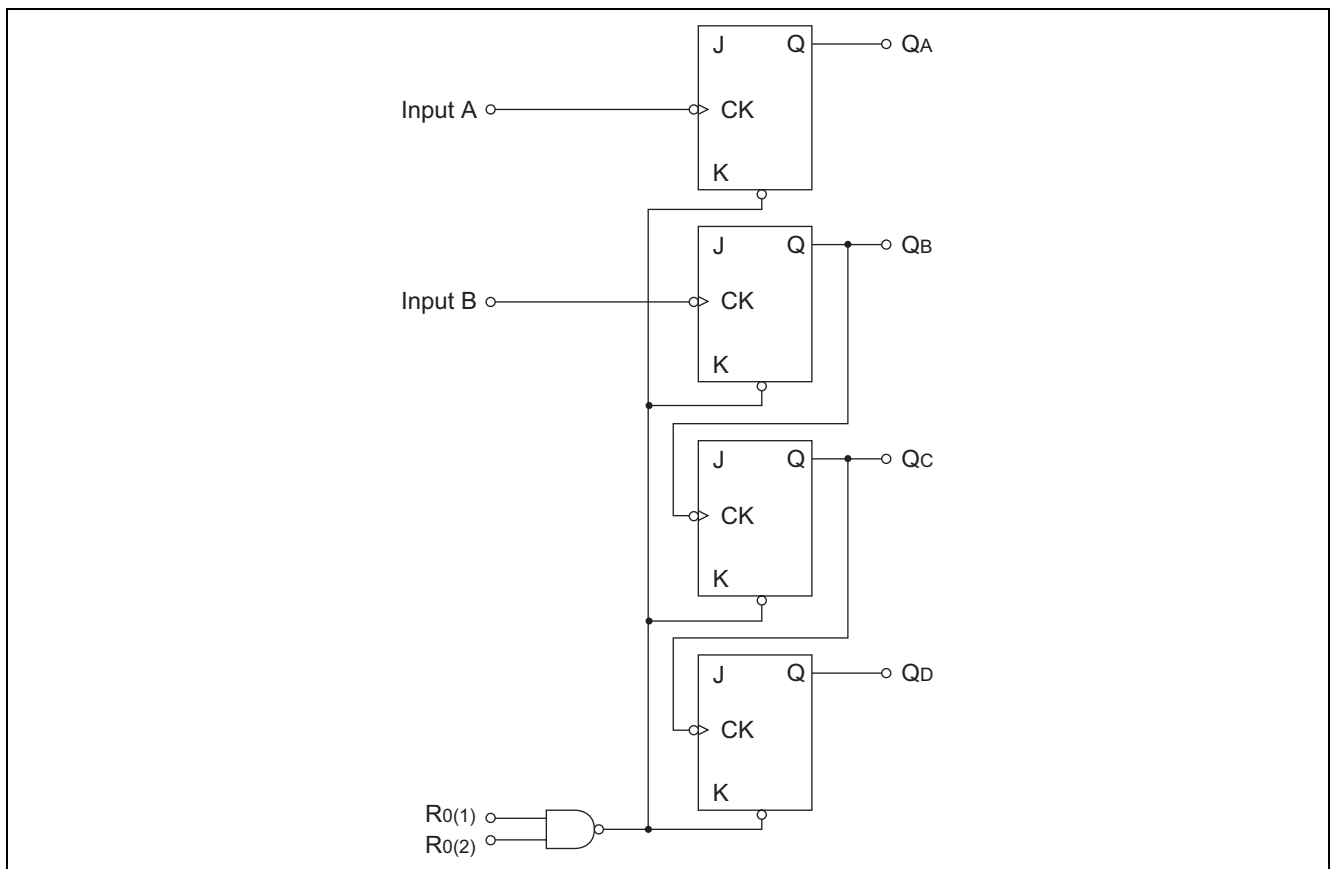
Reset Input		Outputs			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

BCD Count Sequence

Count	Outputs			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes: 1. H; high level, L; low level, X; irrelevant
 2. Output Q_A is connected to input B.

Block Diagram



Absolute Maximum Ratings

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7	V
Input voltage	R_O Inputs	V_{IN}	7	V
	A, B Inputs		5.5	V
Power dissipation		P_T	400	mW
Operating temperature		T_{opr}	-20 to +75	°C
Storage temperature		T_{stg}	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	μA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	-20	25	75	°C
Count frequency	A input	f_{count}	0	—	32	MHz
	B input		0	—	16	
Pulse width	A input	t_w	15	—	—	ns
	B input		30	—	—	
	Reset inputs		15	—	—	
Setup time		t_{su}	25	—	—	ns

Electrical Characteristics

($T_a = -20$ to $+75$ °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V_{IH}	2.0	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	—	—	V	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$	
		V_{OL}	—	—	0.4	V	$I_{OL} = 4\text{ mA}^{**}$	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$
			—	—	0.5		$I_{OL} = 8\text{ mA}^{**}$	
Input current	Any Reset	I_{IH}	—	—	20	μA	$V_{CC} = 5.25\text{ V}$, $V_I = 2.7\text{ V}$	
	A input		—	—	40			
	B input		—	—	40			
	Any Reset	I_{IL}	—	—	-0.4	mA	$V_{CC} = 5.25\text{ V}$, $V_I = 0.4\text{ V}$	
	A input		—	—	-2.4			
	B input		—	—	-1.6			
	Any Reset	I_I	—	—	0.1	mA	$V_I = 7\text{ V}$	$V_{CC} = 5.25\text{ V}$
	A input		—	—	0.2		$V_I = 5.5\text{ V}$	
	B input		—	—	0.2			
Short-circuit output current		I_{OS}	-20	—	-100	mA	$V_{CC} = 5.25\text{ V}$	
Supply current***		I_{CC}	—	9	15	mA	$V_{CC} = 5.25\text{ V}$	
Input clamp voltage		V_{IK}	—	—	-1.5	V	$V_{CC} = 4.75\text{ V}$, $I_{IN} = -18\text{ mA}$	

Notes: * $V_{CC} = 5$ V, $T_a = 25$ °C

** Q_A output is tested at specified I_{OL} plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

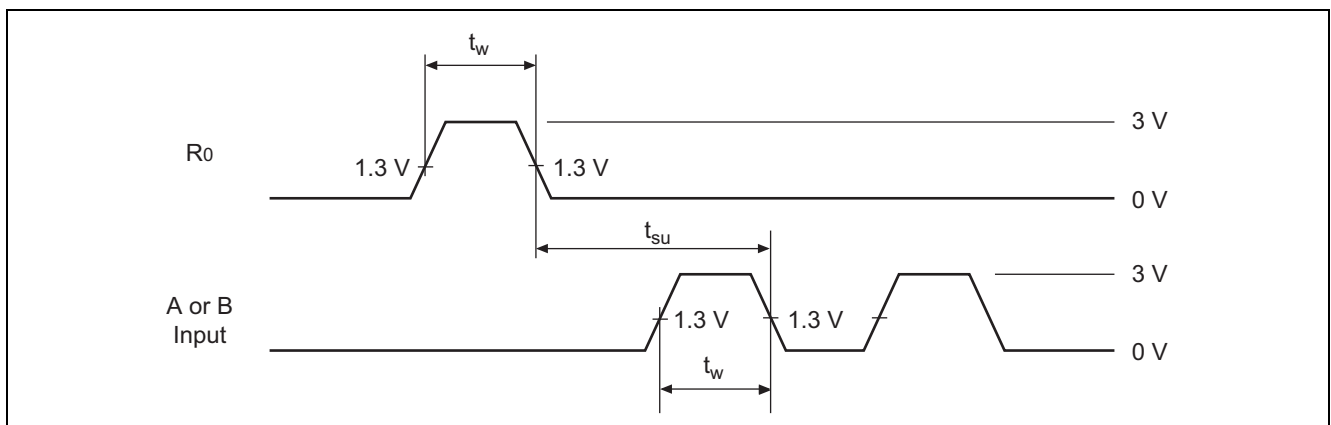
*** I_{CC} is measured with all outputs open, both R_O inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

Switching Characteristics

(V_{CC} = 5 V, T_a = 25°C)

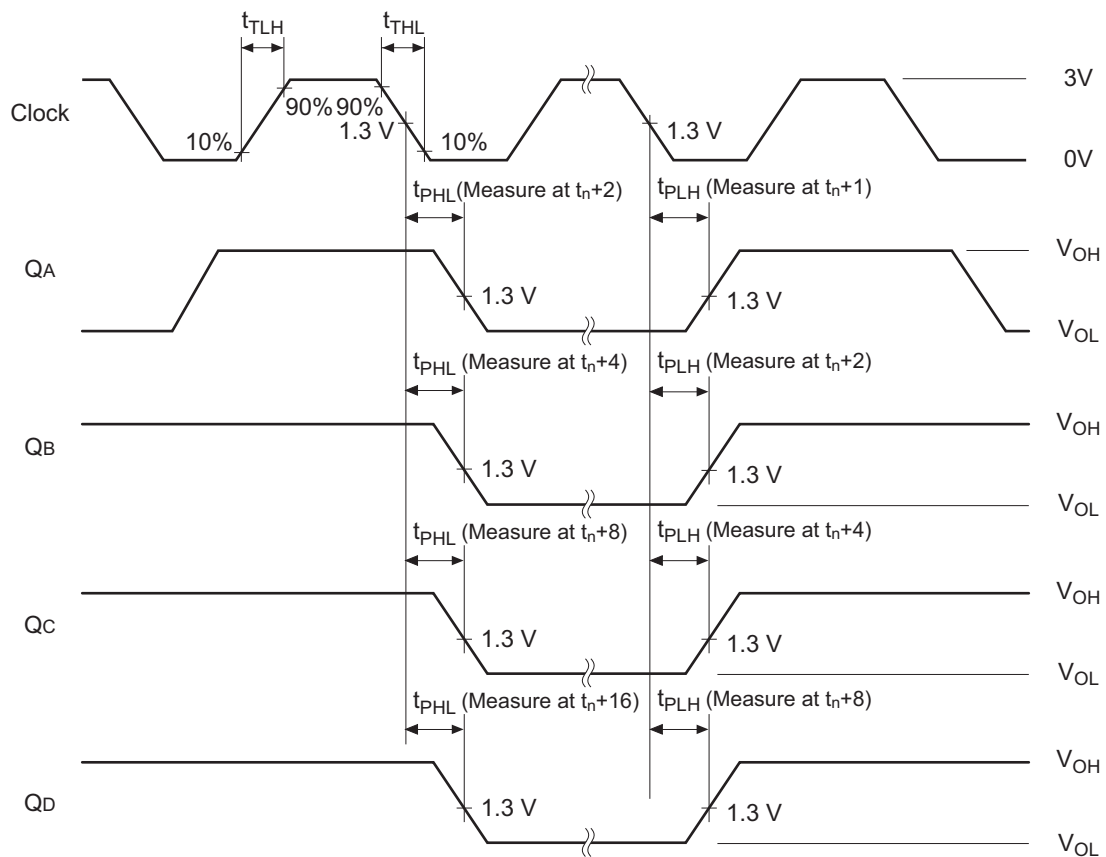
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	$f_{\max}$	A	Q _A	32	42	—	MHz	C _L = 15 pF, R _L = 2 kΩ
		B	Q _B	16	—	—		
Propagation delay time	t _{PLH}	A	Q _A	—	10	16	ns	
	t _{PHL}			—	12	18		
	t _{PLH}	A	Q _D	—	46	70	ns	
	t _{PHL}			—	46	70		
	t _{PLH}	B	Q _B	—	10	16	ns	
	t _{PHL}			—	14	21		
	t _{PLH}	B	Q _C	—	21	32	ns	
	t _{PHL}			—	23	35		
	t _{PLH}	B	Q _D	—	34	51	ns	
	t _{PHL}			—	34	51		
t _{PHL}	Set-to-0	Q _A to Q _D	—	26	40	ns		

Timing Method



Waveforms 1

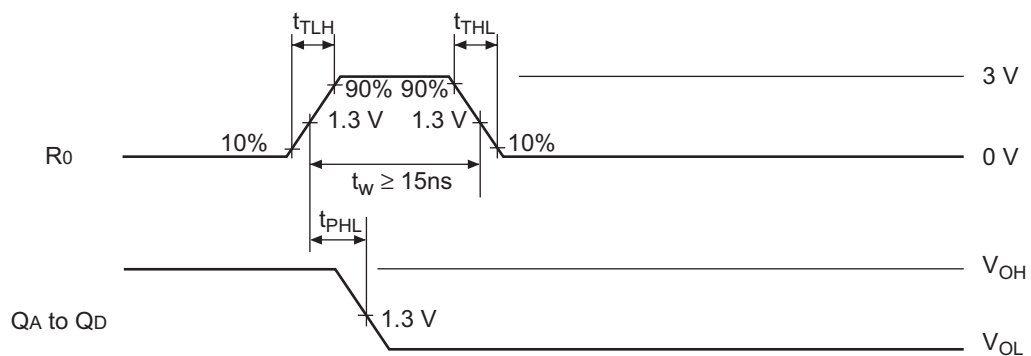
f_{max} , t_{PLH} , t_{PHL} , (Clock→Q)



- Notes:
1. Clock input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle = 50% and : for f_{max} , $t_{TLH} = t_{THL} \leq 2.5$ ns.
 2. t_n is reference bit time when all outputs are low.

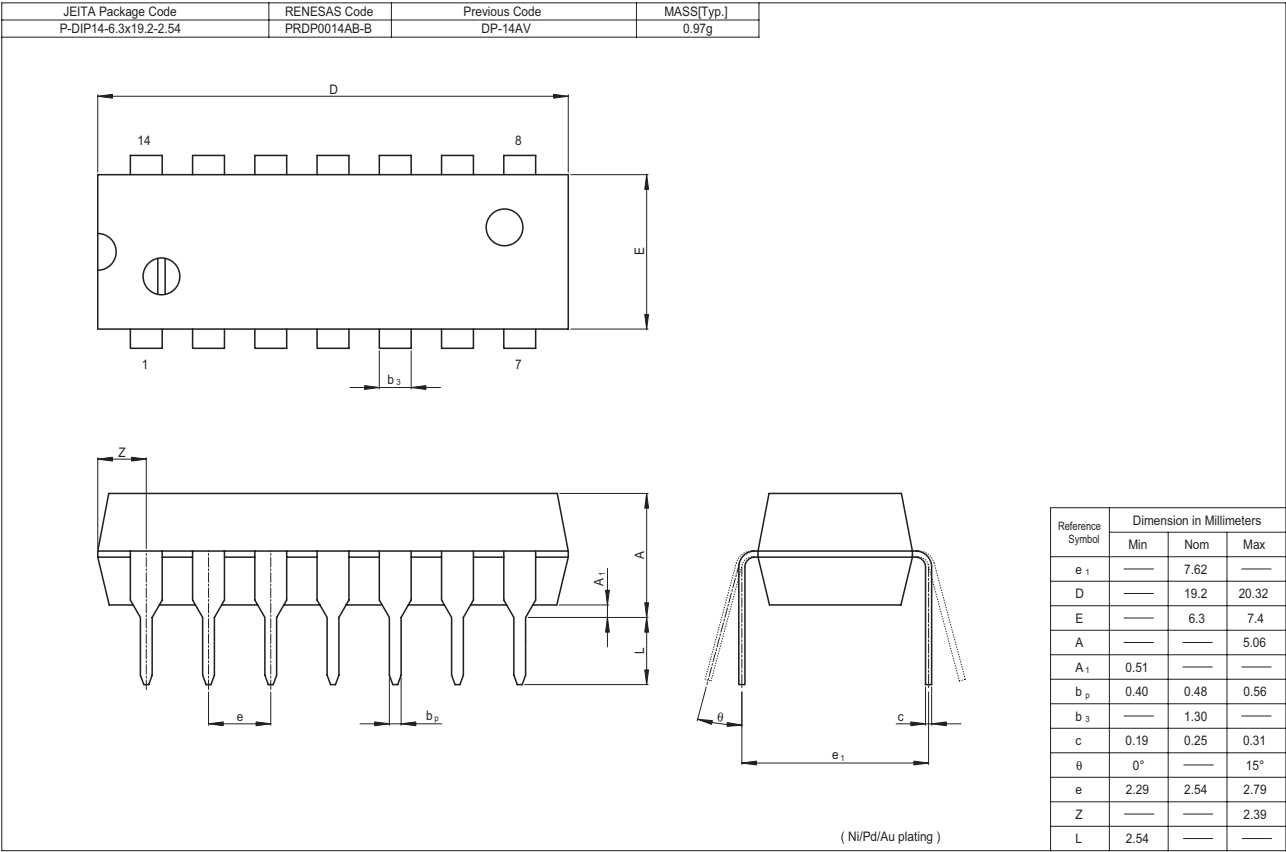
Waveforms 2

t_{PHL} , ($R_0 \rightarrow Q$)



Note: $t_{TLH} \leq 15$ ns, $t_{THL} \leq 5$ ns

Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510