MCP2021/2/1P/2P

LIN Transceiver with Voltage Regulator

Features:

- The MCP2021/2/1P/2P are Compliant with LIN Bus Specifications 1.3, 2.1 and are Compliant to SAE J2602-2
- Support Baud Rates up to 20 kBaud with LIN-compatible Output Driver
- 43V Load Dump Protected
- Very Low EMI Meets Stringent OEM Requirements
- Wide Supply Voltage, 6.0V-18.0V Continuous:
  - Maximum input voltage of 30V
- Extended Temperature Range: -40 to +125°C
- Interface to PIC® EUSART and Standard USARTs
- Local Interconnect Network (LIN) Bus Pin:
  - Internal pull-up resistor and diode
  - Protected against ground shorts
  - Protected against loss of ground
  - High-current drive
- Automatic Thermal Shutdown
- On-Chip Voltage Regulator:
  - Output voltage of 5.0V with tolerances of ±3% overtemperature range
  - Available with alternate output voltage of 3.3V with tolerances of ±3% overtemperature range
  - Maximum continuous input voltage of 30V
  - Internal thermal overload protection
  - Internal short circuit current limit
  - External components limited to filter capacitor and load capacitor
- Two Low-Power modes:
  - Receiver On, Transmitter Off, Voltage Regulator On (≅ 85 µA)
  - Receiver Monitoring Bus, Transmitter Off, Voltage Regulator Off (≅ 16 µA)

Description:

The MCP2021/2/1P/2P provides a bidirectional, half-duplex communication physical interface to automotive and industrial LIN systems that meets the LIN bus specification Revision 2.1 and SAE J2602-2. The devices incorporate a voltage regulator with 5V at 50 mA or 3.3V at 50 mA regulated power-supply outputs.

The regulator is short-circuit protected, and is protected by an internal thermal shutdown circuit. The device has been specifically designed to operate in the automotive operating environment and will survive all specified transient conditions while meeting all of the stringent quiescent current requirements.

The MCP2021/2/1P/2P family of devices includes the following packages.

8-pin PDIP, DFN and SOIC packages:

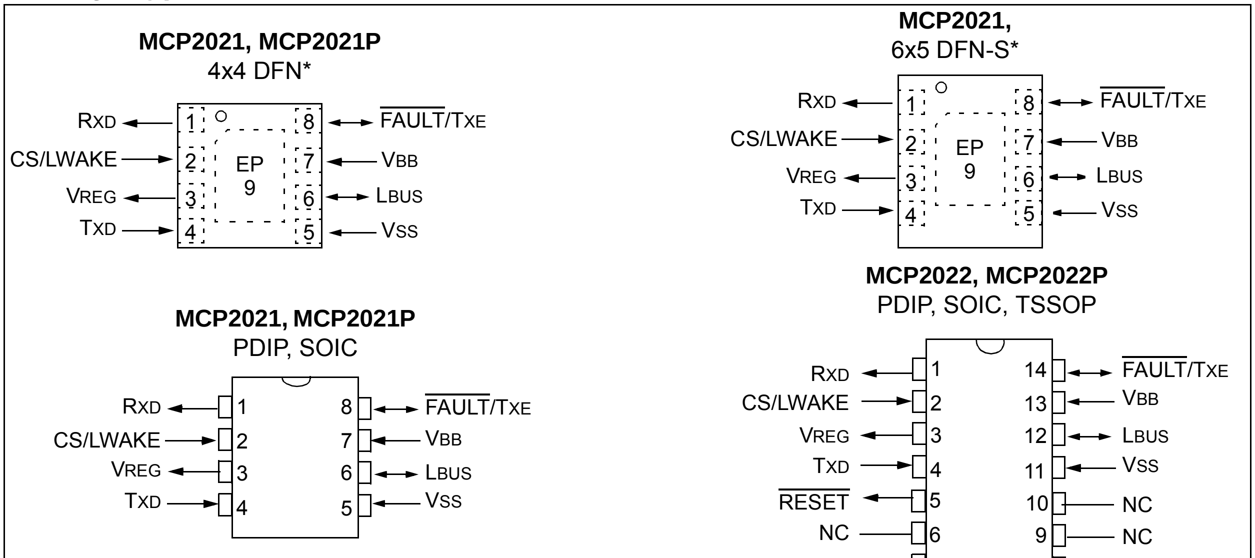
- MCP2021-330, LIN-compatible driver, 8-pin, 3.3V regulator, wake up on dominant level of LBUS
- MCP2021-500, LIN-compatible driver, 8-pin, 5.0V regulator, wake up on dominant level of LBUS
- MCP2021P-330, LIN-compatible driver, 8-pin, 3.3V regulator, wake up at falling edge of LBUS voltage
- MCP2021P-500, LIN-compatible driver, 8-pin, 5.0V regulator, wake up at falling edge of LBUS voltage

14-pin PDIP, TSSOP and SOIC packages with $\overline{\text{RESET}}$ output:

- MCP2022-330, LIN-compatible driver, 14-pin, 3.3V regulator, $\overline{\text{RESET}}$ output, wake up on dominant level of LBUS
- MCP2022-500, LIN-compatible driver, 14-pin, 5.0V regulator, $\overline{\text{RESET}}$ output, wake up on dominant level of LBUS
- MCP2022P-330, LIN-compatible driver, 14-pin, 3.3V regulator, $\overline{\text{RESET}}$ output, wake up at falling edge of LBUS voltage
- MCP2022P-500, LIN-compatible driver, 14-pin, 5.0V regulator, $\overline{\text{RESET}}$ output, wake up at falling edge of LBUS voltage

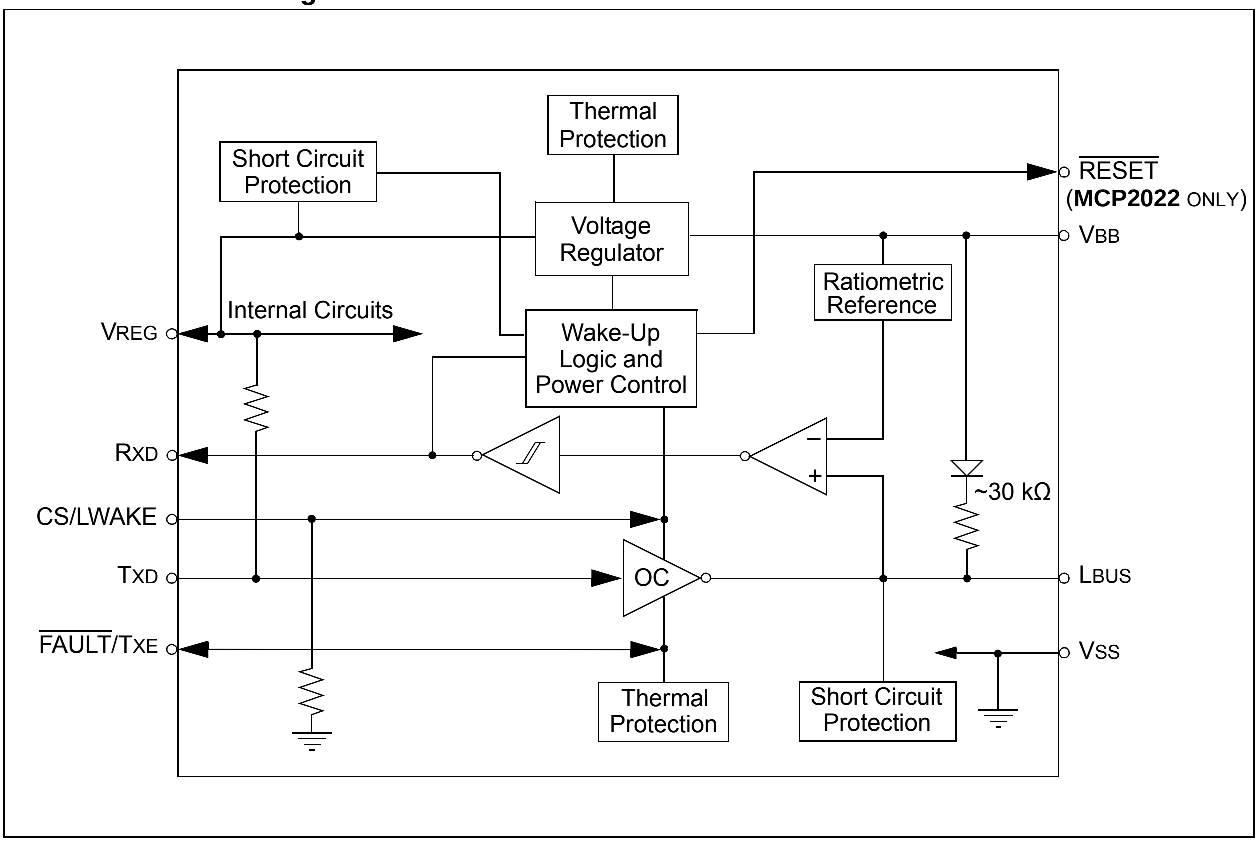
LOCAL INTERCONNECT NETWORK

Package Types

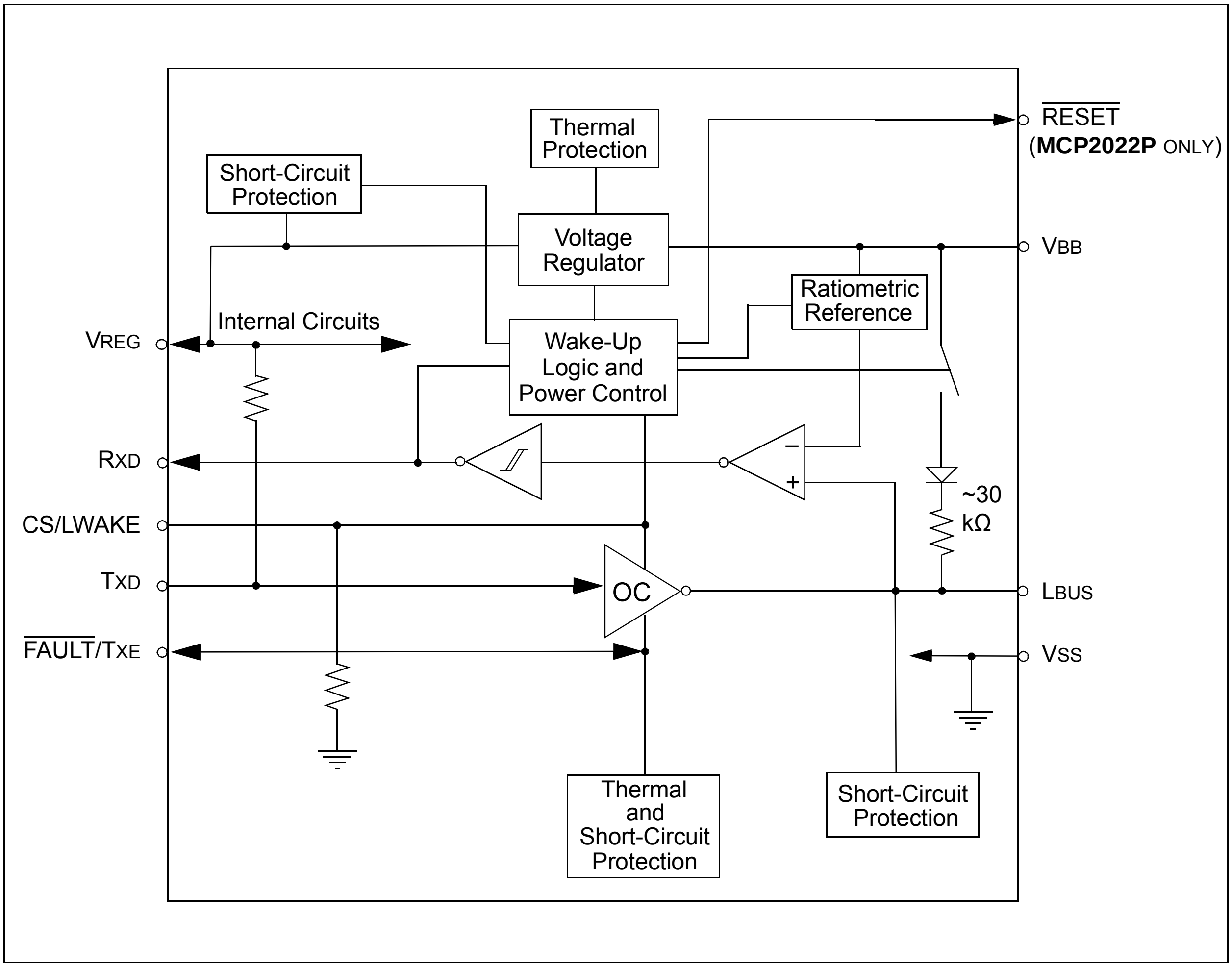


* Includes Exposed Thermal Pad (EP); see Table 1-2.

MCP2021/2 Block Diagram



MCP2021P/2P Block Diagram



NOTES:

1.0 DEVICE OVERVIEW

The MCP2021/2/1P/2P provides a physical interface between a microcontroller and a LIN half-duplex bus. It is intended for automotive and industrial applications with serial bus speeds up to 20 Kbaud.

The MCP2021/2/1P/2P provides a half-duplex, bidirectional communications interface between a microcontroller and the serial network bus. This device will translate the CMOS/TTL logic levels to LIN-level logic, and vice versa.

The LIN specification 2.0 requires that the transceiver(s) of all nodes in the system be connected via the LIN pin, referenced to ground, and with a maximum external termination resistance load of 510Ω from LIN bus to battery supply. The 510Ω corresponds to one Master and sixteen Slave nodes.

The MCP2021/2/1P/2P-500 provides a +5V, 50 mA, regulated power output. The regulator uses an LDO design, is short-circuit protected, and will turn the regulator output off if it falls below 3.5V.

The MCP2021/2/1P/2P also includes thermal-shutdown protection.

The regulator is specifically designed to operate in the automotive environment and will survive +43V load dump transients, double-battery jumps, and reverse battery connections when a reverse blocking diode is used. The other members of the MCP2021/2/1P/2P-330 family output +3.3V at 50 mA with a turn-off voltage of 2.5V. (See **Section 1.6 "Internal Voltage Regulator"**).

MCP2021/2 wakes from Power-Down mode on a dominant level on LBUS. MCP2021P/2P wakes at a transition from recessive level to dominant level on LBUS.

1.1 Optional External Protection

1.1.1 REVERSE BATTERY PROTECTION

An external reverse-battery-blocking diode should be used to provide polarity protection (see Figure 1-6).

1.1.2 TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V transient suppressor (TVS) diode, between VBB and ground, with a 50Ω transient protection resistor (RTP) in series with the battery supply and the VBB pin, protect the device from power transients (see Figure 1-6) and ESD events. While this protection is optional, it is considered good engineering practice. The resistor value is chosen according to Equation 1-1.

EQUATION 1-1:

$$R_{TP} \le (V_{BB_{min}} - 5.5) / 250\ mA.$$
$$5.5V = V_{UVLO} + 1.0V,$$
250 mA is the peak current at Power-On when $V_{BB} = 5.5V$

1.2 Internal Protection

1.2.1 ESD PROTECTION

For component-level ESD ratings, please refer to the **Section 2.1 "Absolute Maximum Ratings†"**.

1.2.2 GROUND LOSS PROTECTION

The LIN Bus specification states that the LIN pin must transition to the recessive state when ground is disconnected. Therefore, a loss of ground effectively forces the LIN line to a high-impedance level.

1.2.3 THERMAL PROTECTION

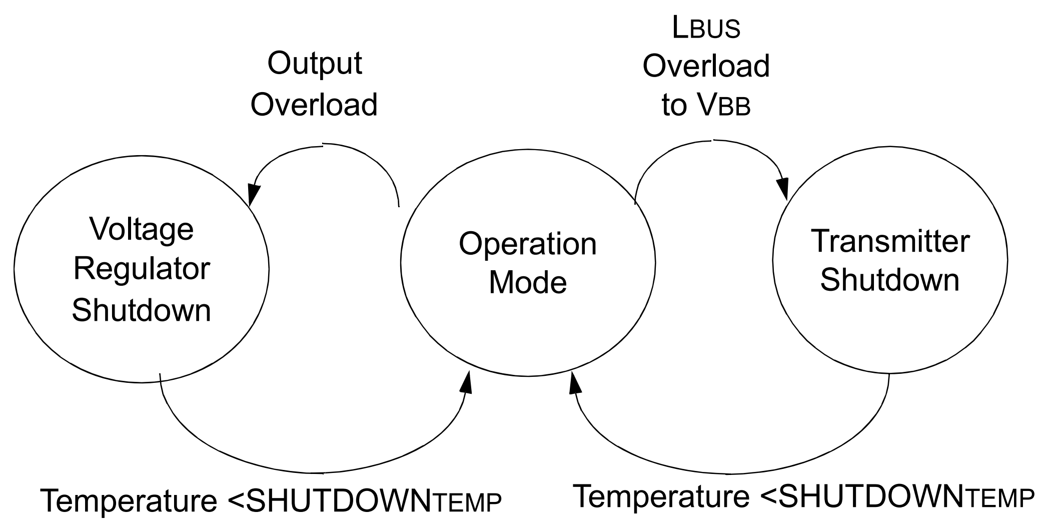
The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter and voltage regulator if it detects a thermal overload.

There are three causes for a thermal overload. A thermal shut down can be triggered by any one, or a combination of, the following thermal overload conditions:

- Voltage regulator overload
- LIN bus output overload
- Increase in die temperature due to increase in environmental temperature

Driving the TXD and checking the RXD pin makes it possible to determine whether there is a bus contention (i.e., RXD = low, TXD = high) or a thermal overload condition (i.e., RXD = high, TXD = low).

FIGURE 1-1: THERMAL SHUTDOWN STATE DIAGRAMS



1.3 Modes of Operation

For an overview of all operational modes, please refer to Table 1-1.

1.3.1 POWER-ON RESET MODE

Upon application of VBB, the device enters Power-On Reset mode (POR). During this mode, the part maintains the digital section in a Reset mode and waits until the voltage on pin VBB rises above the “ON” threshold (typically 5.75V) to enter to the Ready mode. If during the operation, the voltage on pin VBB falls below the “OFF” threshold (typically 4.25V), the part comes back to the POR mode.

1.3.2 POWER-DOWN MODE

In Power-Down mode, the transmitter and the voltage regulator are off. Only the receiver wake-up from the LIN bus section, and the CS/LWAKE pin wake-up circuits, are in operation. This is the lowest power mode.

If pin CS/LWAKE goes to a high level during Power-Down mode, the device immediately enters Ready mode and enables the voltage regulator; and after the output has stabilized (approximately 0.3 ms to 1.2 ms), the device goes to Operation mode or Transmitter-Off mode (see Figure 1-2 for MCP2021/2 and Figure 1-4 for MCP2021P/2P).

Note:	The above time interval <1.2 ms assumes 12V VBB input and no thermal shutdown event.

LIN bus activity will also change the device from Power-Down mode to Ready mode. MCP2021/2 wakes up on the dominant level of the LIN bus, and MCP2021P/2P on a falling edge that follows a dominant level lasting 20 µs of time.

The Power-Down mode can be reached through either Operation mode or Transmitter-Off mode.

1.3.3 READY MODE

Upon entering Ready mode, the voltage regulator and receiver-threshold-detect circuit are powered up. The transmitter remains in an OFF state. The device is ready to receive data as soon as the regulator is stabilized, but not to transmit. If a microcontroller is being driven by the voltage regulator output, it will go through a POR and initialization sequence. The LIN pin is in the recessive state for MCP2021/2 and in floating state for MCP2021P/2P.

The device will stay in Ready mode until the output of the voltage regulator has stabilized and the CS/LWAKE pin is true (‘1’). After VREG is stable and CS/LWAKE is high, MCP2021/2 will enter Operation mode; and MCP2021P/2P will enter either Operation mode or Transmitter-Off mode, depending on the level of the $\overline{\text{FAULT}}$/TXE pin (refer to Figure 1-4).

1.3.4 OPERATION MODE

In this mode, all internal modules are operational.

The device will go into the Power-Down mode on the falling edge of CS/LWAKE.

For the MCP2021P/2P devices, the pull-up resistor is switched on only in this mode.

1.3.5 TRANSMITTER-OFF MODE

Whenever the $\overline{\text{FAULT}}$/TXE signal is low, or permanent dominant on TXD/LBUS is detected, the LBUS transmitter is off.

The transmitter may be re-enabled whenever the $\overline{\text{FAULT}}$/TXE signal returns high, either by removing the internal Fault condition or when the CPU returns the $\overline{\text{FAULT}}$/TXE high. The transmitter will not be enabled if the $\overline{\text{FAULT}}$/TXE pin is brought high when the internal fault is still present.

If TX-OFF mode is caused by TXD/LBUS permanent dominant level, the transmitter can recover when the permanent dominant status disappears.

The transmitter is also turned off whenever the voltage regulator is unstable or recovering from a fault. This prevents unwanted disruption of the bus during times of uncertain operation.

1.3.6 REMOTE WAKE-UP

The Remote Wake-Up sub-module observes the LBUS in order to detect bus activity. Bus activity is detected when the voltage on the LBUS stays below a threshold of approximately 0.4 VBB for a typical duration of at least 20 µs. The MCP2021/2 device is level sensitive to LBUS. Dominant level longer than 20 µs will cause the device to leave the Power-Down mode. The MCP2021P/2P device is falling-edge sensitive to LBUS. Only the LBUS transition from recessive to dominant, followed by at least 20 µs dominant level, can wake up the device. Putting CS/LWAKE to high level also wakes up the device. Refer to Figure 1-2 and Figure 1-3.

1.3.7 DIFFERENCE DETAILS BETWEEN MCP2021/2 AND MCP2021P/2P

The MCP202XP is a minor variation of the MCP202X device that adds improved state machine control, as well as the ability to disconnect the internal 30kΩ pull-up between LIN and VBB in all modes except normal operation. These changes allow the system designer to better handle Fault conditions and reduce the overall system current consumption. The differences between the two device versions are as follows:

1. Switchable LIN-VBB Pull-Up Resistor:

   On the MCP202XP device, the internal 30kΩ pull-up resistor is disconnected in all modes except Operation mode. On the MCP202X device, this pull-up resistor is always connected. (See the MCP2021/2 Block Diagram and the MCP2021P/2P Block Diagram for details.)

2. Power-Down Wake-up on LIN Traffic:

   The MCP202XP device requires a LIN falling edge to generate a valid Wake condition, due to bus traffic. The MCP202X device will generate a Wake anytime LIN is at a valid dominant level. Because of this, if the LIN bus becomes permanently shorted, it becomes impossible to place the MCP202X in a low-power state.

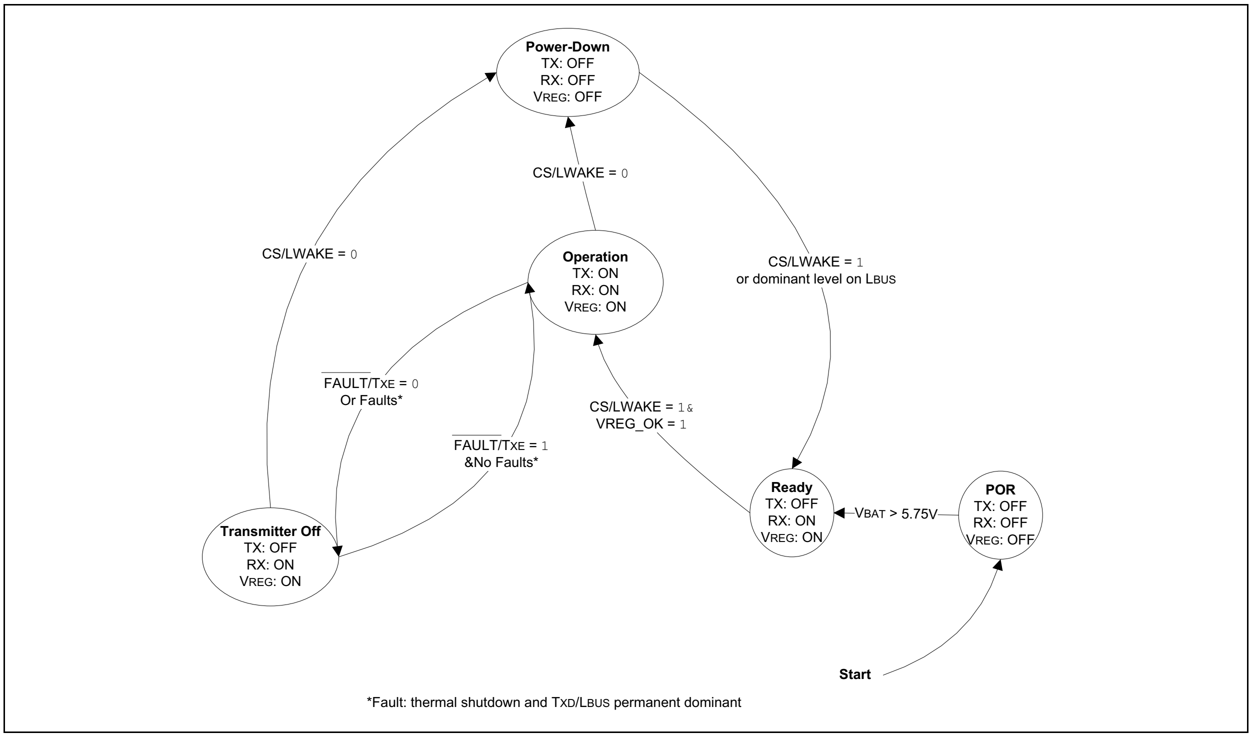
3. State Machine Options:

   The MCP202XP device is able to enter Transmitter Off mode from Ready mode without transitioning through Operation mode. The MCP202X device must enter Operation mode from Ready mode. (see State Machine Diagrams, Figure 1-2 and Figure 1-3 for details). This capability allows the system designer to monitor the bus in Ready mode to determine if the system should transition to normal operation and connect the internal pull-up, or if Ready mode was reached due to an invalid condition. In the case of an invalid condition, the MCP202XP device can be placed into Power-Down mode without connecting the internal pull-up and waking other nodes on the LIN Bus network.

Note:	To enter Transmitter Off, the system must set TXE 'low' before pulling CS high (see Figure 1-5). Otherwise, if CS is pulled high first, the MCP202XP will enter Operation mode due to the internal pull-up on TXE.

To properly take advantage of the device differences, the system designer is required to implement some microcontroller code to the power-up routine. This code will monitor the status of the LIN bus to determine how to respond to the dominant signal. It will also determine if the local LIN node needs to respond or can 'Listen Only'. If the local LIN node does not need to respond, it can enter Transmitter Off mode, disconnecting the 30 kΩ pull-up, reducing module current while still maintaining the ability to properly receive all valid LIN messages.

FIGURE 1-2: MCP2021/2 OPERATIONAL MODES STATE DIAGRAM



Note:	While the device is in shutdown, TXD should not be actively driven high or it may power internal logic through the ESD diodes and may damage the device.

FIGURE 1-3: MCP2021P/2P OPERATIONAL MODES DIAGRAMS

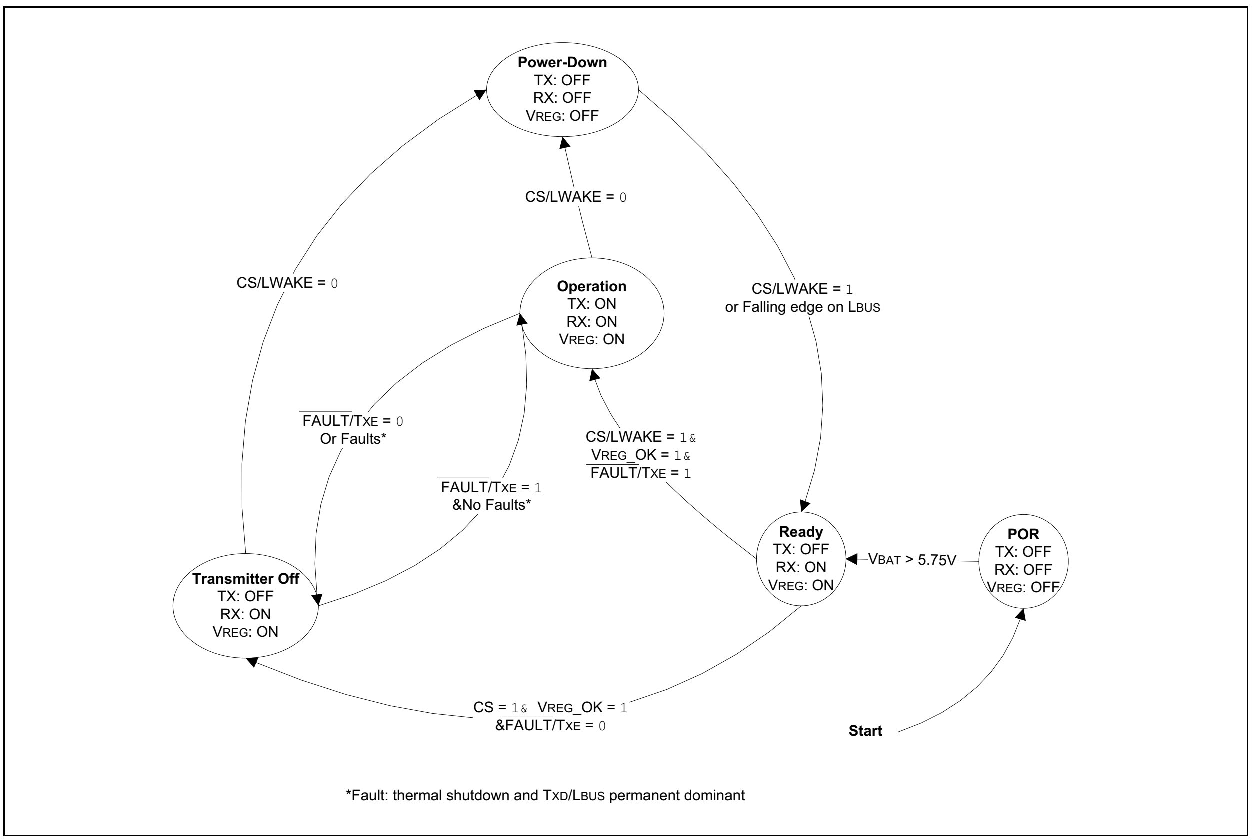


FIGURE 1-4: MCP2021P/2P WAKE-UP DUE TO BUS DISCONNECTING

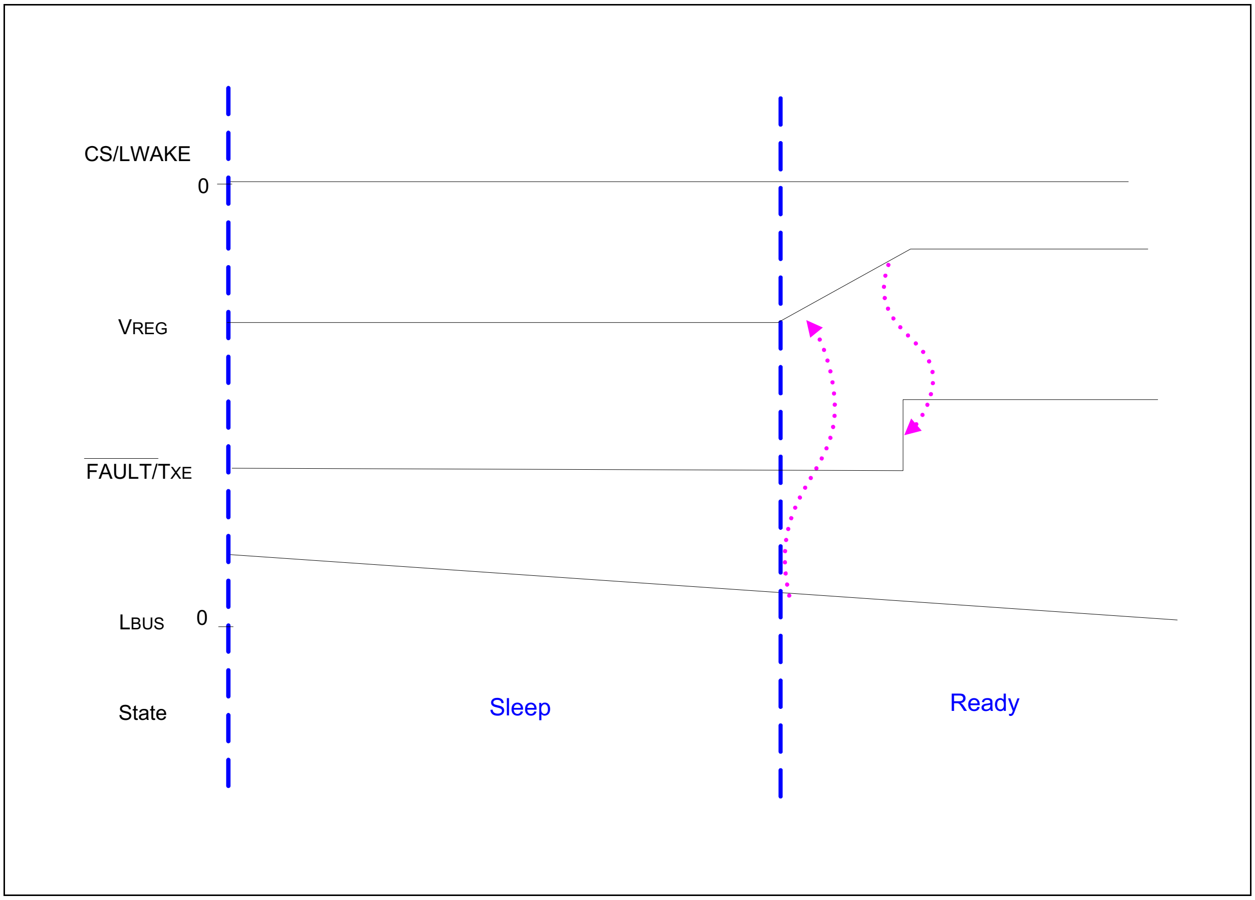


FIGURE 1-5: FORCED POWER-DOWN MODE SEQUENCE FOR MCP2021P/2P

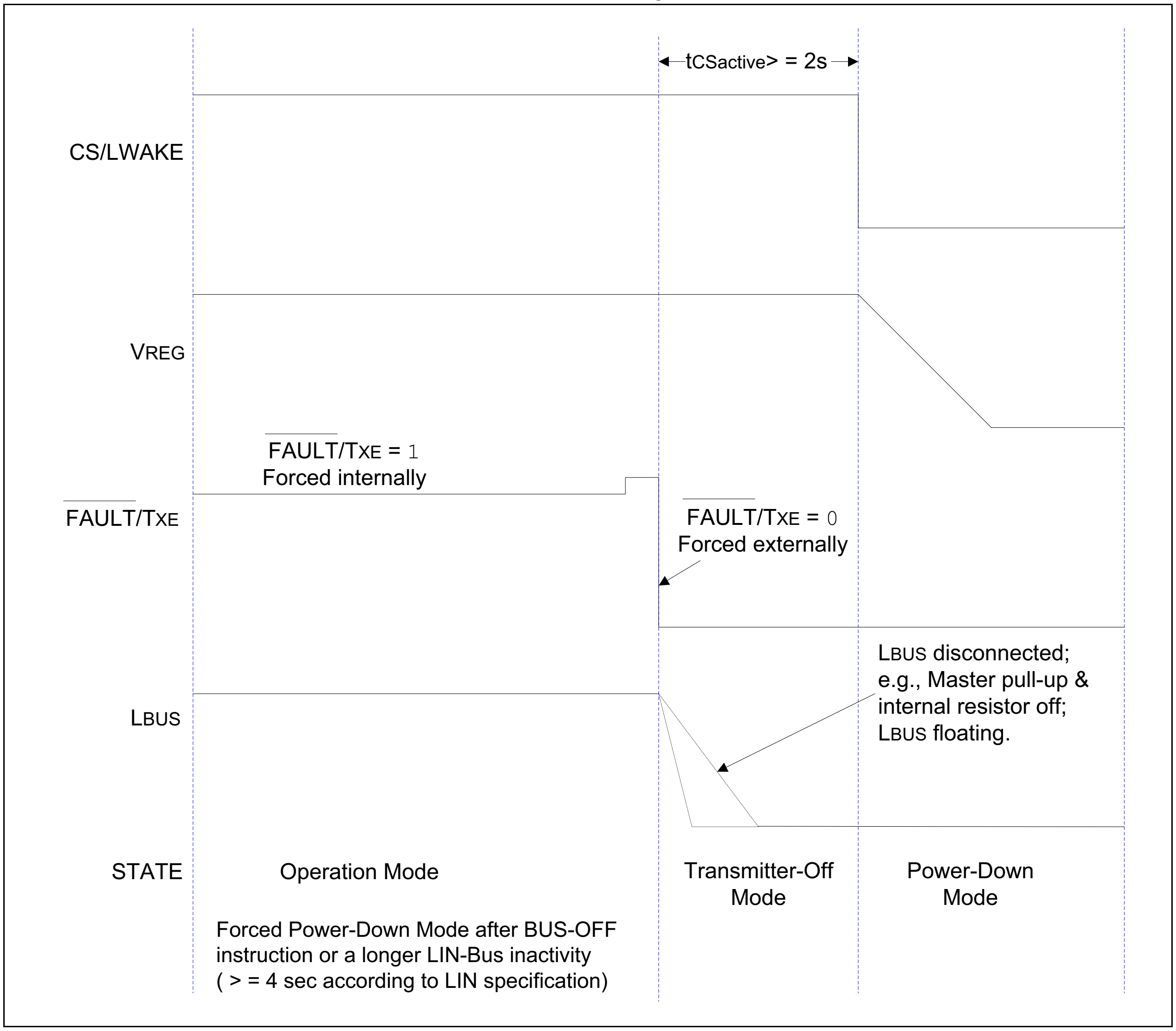


TABLE 1-1: OVERVIEW OF OPERATIONAL MODES

State	Transmitter	Receiver	Voltage Regulator	Operation	Comments
POR	OFF	OFF	OFF	Read V_{BB}; if $V_{BB} > 5.75V$, proceed to Ready mode	
Ready	OFF	ON	ON	**MCP2021/2**: If CS/LWAKE is high level, then proceed to Operation mode. **MCP2021P/2P**: If CS/LWAKE is high level and $\overline{\text{FAULT}}/T_{XE}$ is high level, then proceed to Operation mode. If CS/LWAKE is high level and $\overline{\text{FAULT}}/T_{XE}$ is low level, then proceed to TXOFF mode.	Bus OFF state
Operation	ON	ON	ON	If CS/LWAKE is low level, then proceed to Power-Down mode. If $\overline{\text{FAULT}}/T_{XE}$ is low level or T_{XD}/L_{BUS} permanent dominant is detected, then proceed to Transmitter-Off mode.	Normal Operation mode
Power-Down	OFF	Activity Detect	OFF	On LIN bus falling, go to Ready mode. On CS/LWAKE high level, go through Ready mode; then, to either operation or Transmitter-Off mode (refer to Figure 1-2 and Figure 1-3).	Low-Power mode
Transmitter-Off	OFF	ON	ON	If CS/LWAKE is low level, then proceed to Power-Down mode. If $\overline{\text{FAULT}}/T_{XE}$ is high, then proceed to Operation mode.	

1.4 Pin Descriptions

TABLE 1-2: PINOUT DESCRIPTIONS

Pin Name	Devices			Pin Type	Function
	8-Pin PDIP, SOIC	4x4 DFN 6x5 DFN-S	14-Pin PDIP, SOIC, TSSOP		Normal Operation
RXD	1	1	1	O	Receive Data Output (CMOS)
CS/LWAKE	2	2	2	TTL	Chip Select (TTL)
VREG	3	3	3	O	Power Output
TXD	4	4	4	I	Transmit Data Input (TTL)
VSS	5	5	11	P	Ground
LBUS	6	6	12	I/O	LIN bus (Bidirectional)
NC	—	—	6 – 10	—	No Connection
VBB	7	7	13	P	Battery Supply
$\overline{\text{FAULT}}$/TXE	8	8	14	OD	Fault Detect Output, Transmitter Enable (OD)
$\overline{\text{RESET}}$	—	—	5	OD	$\overline{\text{RESET}}$ Signal Output (OD)
EP	—	9	—	—	Exposed Thermal Pad

Legend: O = Output, P = Power, I = Input, TTL = TTL input buffer, OD = Open-Drain Output

1.4.1 RECEIVE DATA OUTPUT (RXD)

The Receive Data Output pin is a standard CMOS output and follows the state of the LIN pin.

1.4.2 CHIP SELECT PIN (CS/LWAKE)

An internal pull-down resistor will keep the CS/LWAKE pin low. This is done to ensure that no disruptive data will be present on the bus while the microcontroller is executing a POR and I/O initialization sequence. The pin must see a high level to activate the transmitter.

If CS/LWAKE = 0 when the VBB supply is turned on, the device stays in Ready mode (Low-Power mode). In Ready mode, both the receiver and the voltage regulator are on and the LIN transmitter driver is off.

If CS/LWAKE = 1 when the VBB supply is turned on, the device will proceed to either Operation or Transmitter-Off mode (refer to Figure 1-2 and Figure 1-3) after the VREG output has stabilized.

This pin may also be used as a local wake-up input (see Figure 1-6). In this implementation, the microcontroller will set the I/O pin that controls the CS/LWAKE as an high-impedance input. The internal pull-down resistor will keep the input low. An external switch, or other source, can then wake up the transceiver and the microcontroller.

Note:	CS/LWAKE should not be tied directly to VREG as this could force the MCP202X into Operation mode before the microcontroller is initialized.

1.4.3 POWER OUTPUT (VREG)

Positive Supply Voltage Regulator Output pin.

1.4.4 TRANSMIT DATA INPUT (TXD)

The Transmit Data Input pin has an internal pull-up to VREG. The LIN pin is low (dominant) when TXD is low, and high (recessive) when TXD is high.

For extra bus security, TXD is internally forced to ‘1’ when VREG is less than 1.8V (typical).

If the thermal protection detects an overtemperature condition while the signal TXD is low, the transmitter is shut down. The recovery from the thermal shutdown is equal to adequate cooling time.

1.4.5 GROUND PIN (VSS)

Ground pin.

1.4.6 LIN BUS PIN (LBUS)

The bidirectional LIN bus Interface pin is the driver unit for the LIN pin and is controlled by the signal TXD. LIN has an open collector output with a current limitation. To reduce EMI, the edges during the signal changes are slope-controlled. To further reduce radiated emissions, the LBUS pin has corner-rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus, and generates output signal RXD that follows the state of the LBUS. A 1st degree with 1 µs time constant (160 kHz), low-pass input filter is placed to maintain EMI immunity.

1.4.7 NO CONNECTION (NC)

No internal connection.

1.4.8 BATTERY POSITIVE SUPPLY VOLTAGE (VBB)

Battery Positive Supply Voltage pin. This pin is also the input for the internal voltage regulator.

1.4.9 FAULT/TXE

Fault Detect Output and Transmitter Enable Input bidirectional pin.

This pin is an open-drain output. Its state is defined as shown in Table 1-3. The transmitter driver is disabled whenever this pin is low (‘0’), either from an internal Fault condition or by external drive. This allows the transmitter to be placed in an OFF state and still allow the voltage regulator to operate. Refer to Table 1-1.

The FAULT/TXE also signals a mismatch between the TXD input and the LBUS level. This can be used to detect a bus contention. Since the bus exhibits a propagation delay, the sampling of the internal compare is debounced to eliminate false faults.

This pin has an internal pull-up resistor of approximately 750 kΩ. The internal pull-up resistor may be too weak for some applications. We recommend adding a 10 kOhm external pull-up resistor to ensure a logic high level.

> **Note 1:** The FAULT/TXE pin is true (0) whenever the internal circuits have detected a short or thermal excursion and have disabled the LBUS output driver.
>
> **2:** FAULT/TXE is true (0) when VREG not OK and has disabled the LBUS output driver.

The FAULT/TXE pin sampled at a rate faster than every 10 µs.

TABLE 1-3: FAULT/TXE TRUTH TABLE

TXD In	RXD Out	LINBUS I/O	Thermal Override	FAULT/TXE		Definition
				External Input	Driven Output	
L	H	VBB	OFF	H	L	**FAULT**, TXD driven low, LBUS shorted to VBB **(Note 1)**
H	H	VBB	OFF	H	H	**OK**
L	L	GND	OFF	H	H	**OK**
H	L	GND	OFF	H	H	**OK**, data is being received from the LBUS
x	x	VBB	ON	H	L	**FAULT**, transceiver in thermal shutdown
x	x	VBB	x	L	x	**NO FAULT**, the CPU is commanding the transceiver to turn off the transmitter driver

Legend: x = don’t care

Note 1: The FAULT/TXE is valid after approximately 25 µs after TXD falling edge. This is to eliminate false fault reporting during bus propagation delays.

1.4.10 RESET

RESET is an open-drain output pin. This pin reflects an internal signal that tracks the internal system voltage has reached a valid, stable level.

As long as the internal voltage is valid, this pin will keep high-impedance. When the system voltage drops below the minimum required, the voltage regulator will shut down and immediately convert the RESET output to short to GND. A pull-up resistor is needed to change the output to high/low voltage. When connected to a microcontroller input, this can provide a warning that the voltage regulator is shutting down (see Figure 1-2).

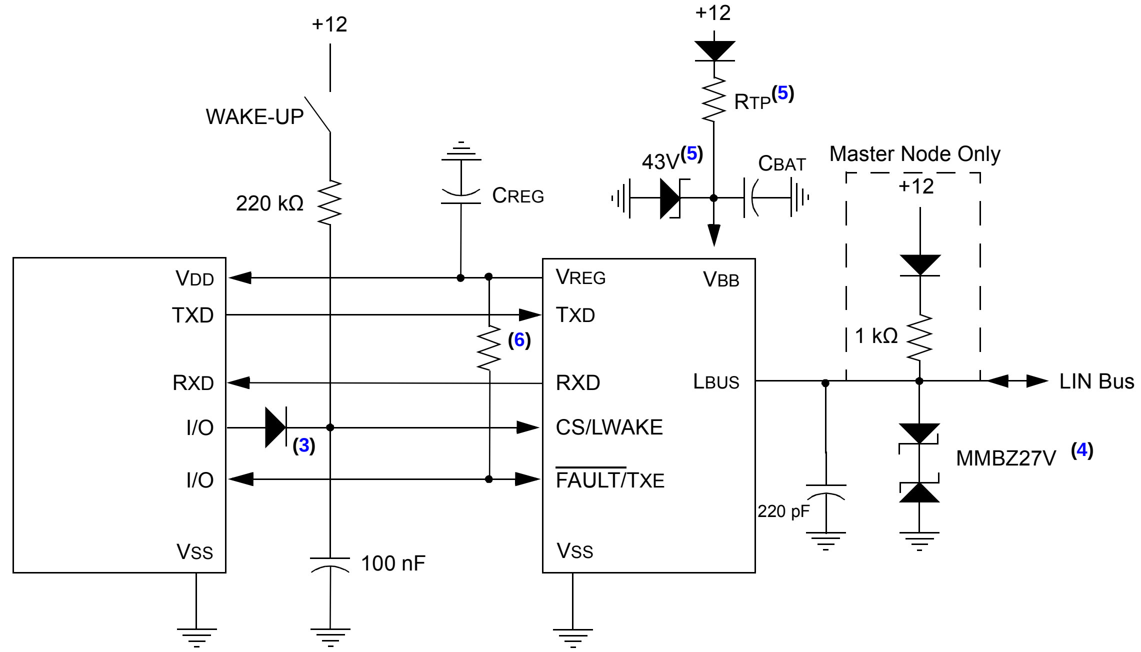
Alternately, it can act as an external brown-out by connecting the RESET output to MCLR (see Figure 1-2). In addition to monitoring the internal voltage, RESET is asserted immediately upon entering the Power-Down mode.

1.4.11 EXPOSED THERMAL PAD (EP)

It is recommended to connect this pad to VSS to enhance electromagnetic immunity and thermal resistance.

1.5 Typical Applications

FIGURE 1-6: TYPICAL MCP2021/MCP2021P APPLICATION



Note 1: Note CREG, the load capacitor, should be ceramic or tantalum rated for extended temperatures, 1.0 – 22 µF. See Figure 2-1 to select the correct ESR.

2: CBAT is the filter capacitor for the external voltage supply.

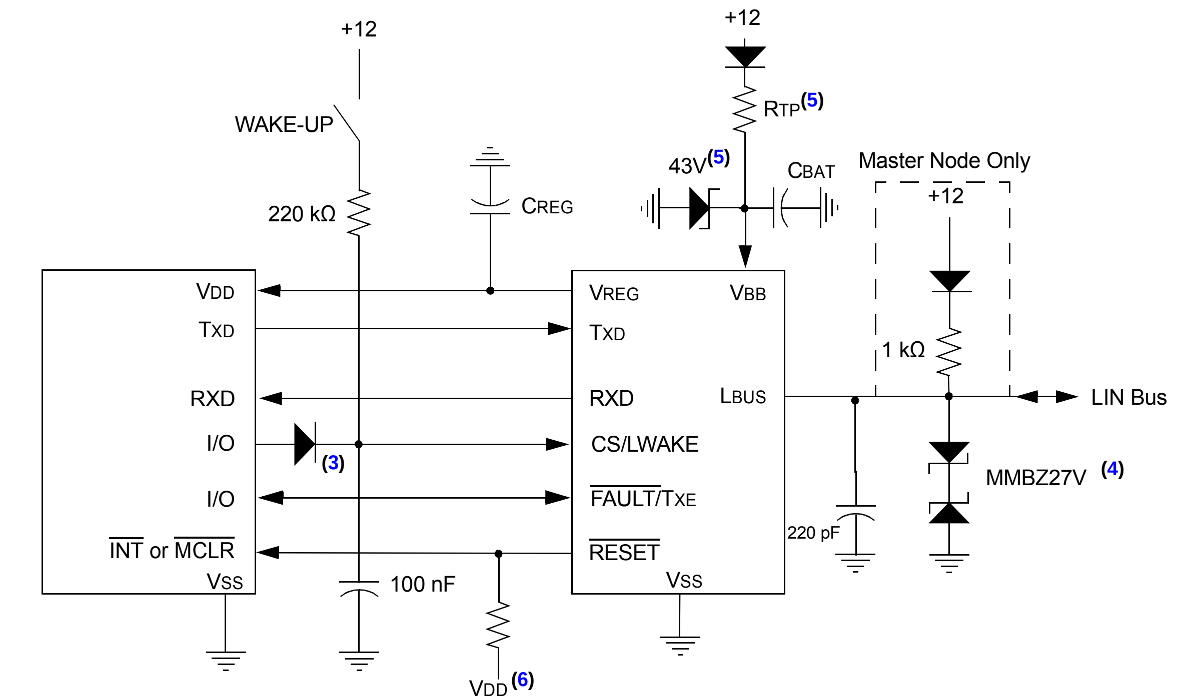
3: This diode is only needed if CS/LWAKE is connected to the VBAT supply.

4: Transient suppressor diode.

5: These components are required for additional load dump protection above 43V.

6: An external 10 kΩ resistor is recommended for some applications.

FIGURE 1-7: TYPICAL MCP2022/MCP2022P APPLICATION



Note 1: Note CREG, the load capacitor, should be ceramic or tantalum rated for extended temperatures, 1.0 – 22 µF. See Figure 2-1 to select the correct ESR.

2: CF is the filter capacitor for the external voltage supply.

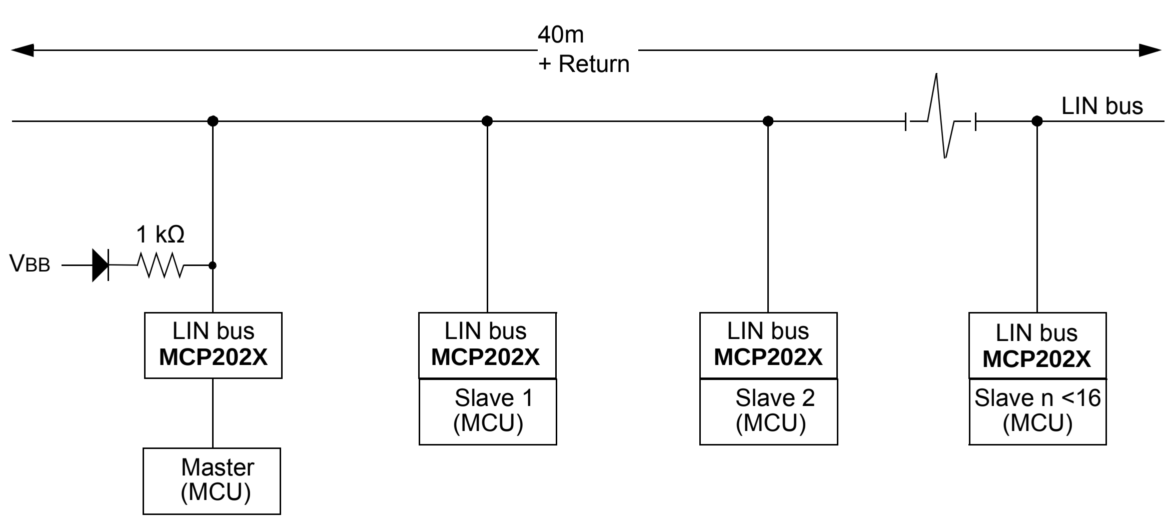
3: This diode is only needed if is connected to the VBAT supply.

4: Transient suppressor diode.

5: These components are required for additional load dump protection above 43V.

6: Required if CPU does not have internal pull-up.

FIGURE 1-8: TYPICAL LIN NETWORK CONFIGURATION



1.6 Internal Voltage Regulator

1.6.1 5.0V REGULATOR

The MCP2021 has a low-drop-out voltage, positive regulator capable of supplying 5.00 V_{DC} ±3% at up to 50 mA of load current, over the entire operating temperature range of -40°C to +125°C. With a load current of 50 mA, the minimum input to output voltage differential required for the output to remain in regulation is typically +0.5V (+1V maximum over the full operating temperature range). Quiescent current is less than 100 µA with a full 50 mA load current when the input to output voltage differential is greater than +3.00V.

Designed for automotive applications, the regulator will protect itself from double-battery jumps and up to +43V load dump transients. The voltage regulator has both short-circuit and thermal-shut-down protection built in.

Regarding the correlation between V_{BB}, V_{REG} and I_{DD}, please refer to Figure 1-10 and Figure 1-11. When the input voltage (V_{BB}) drops below the differential needed to provide stable regulation, the output V_{REG} will track the input down to approximately 3.5V, at which point the regulator will turn off. This will allow microcontrollers with internal POR circuits to generate a clean arming of the POR trip point. The MCP2021 will then monitor V_{BB} and turn on the regulator when V_{BB} rises above 5.75, again.

When the input voltage (V_{BB}) drops below the differential needed to provide stable regulation, the output V_{REG}) will track the input down to approximately +4.25V. The regulator will turn off the output at this point. This will allow PIC microcontrollers with internal POR circuits to generate a clean arming of the POR trip point. The regulator output will stay off until V_{BB} is above +5.75 V_{DC}.

In the start phase, the device must detect at least 5.75V to initiate operation during power-up. In the Power-Down mode, the V_{BB} monitor will be turned off.

> **Note:** The regulator has an overload current limiting of approximately 100 mA. During a short circuit, the V_{REG} is monitored. If V_{REG} is lower than 3.5V, the V_{REG} will turn off. After a recovery time of about three milliseconds, the V_{REG} will be checked again. If there is no short circuit (V_{REG} >3.5V), the V_{REG} will be switched back on.

The regulator has a thermal shutdown. If the thermal protection circuit detects an overtemperature condition, and the signals TXD and RXD are Low, or TXD is High, the regulator will shut down. The recovery from the thermal shutdown is equal to adequate cooling time.

The regulator requires an external output bypass capacitor for stability. See Figure 2-1 for correct capacity and ESR for stable operation.

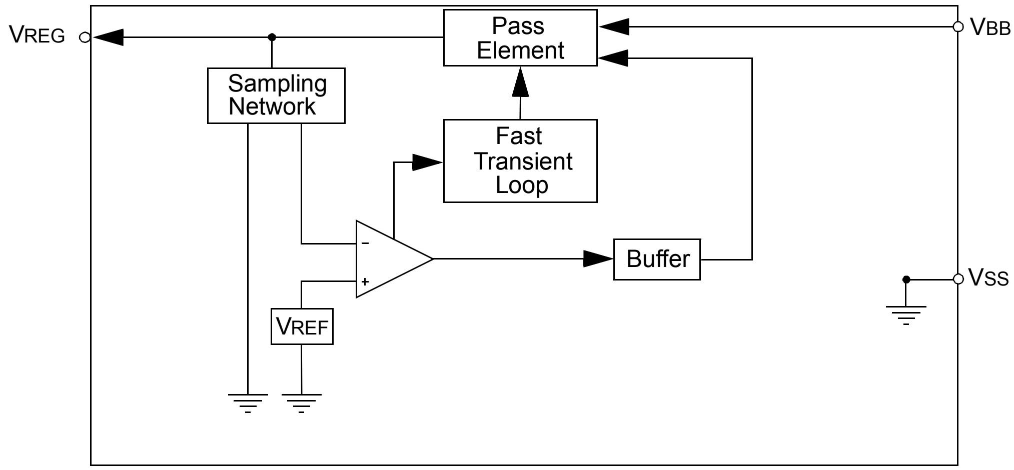
> **Note:** A ceramic capacitor of at least 10 µF or a tantalum capacitor of at least 2.2 µF is recommended for stability.

In worst-case scenarios, the ceramic capacitor may derate by 50%, based on tolerance, voltage and temperature. Therefore, in order to ensure stability, ceramic capacitors smaller than 10 µF may require a small series resistance to meet the ESR requirements, as shown in Table 1-4.

TABLE 1-4: RECOMMENDED SERIES RESISTANCE FOR CERAMIC CAPACITORS

Resistance	Capacitor
Ω	1 µF
0.47Ω	2.2 µF
0.22Ω	4.7 µF
0.1Ω	6.9 µF

FIGURE 1-9: VOLTAGE REGULATOR BLOCK DIAGRAM



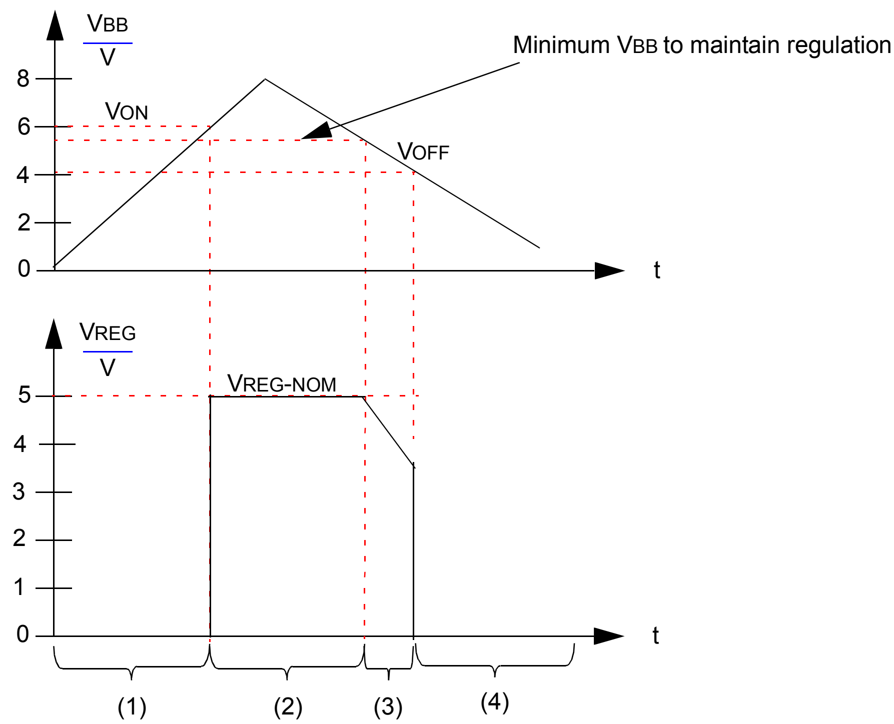
1.6.2 3.3V REGULATOR

A metal option provides for a alternate 3.30 VDC ±3% at up to 50 mA of load current over the entire operating temperature range of -40°C to +125°C. All specifications given above for the 5.0V operation apply except for any difference noted here.

The same input tracking of 4.25V applies the 3.3V regulator.

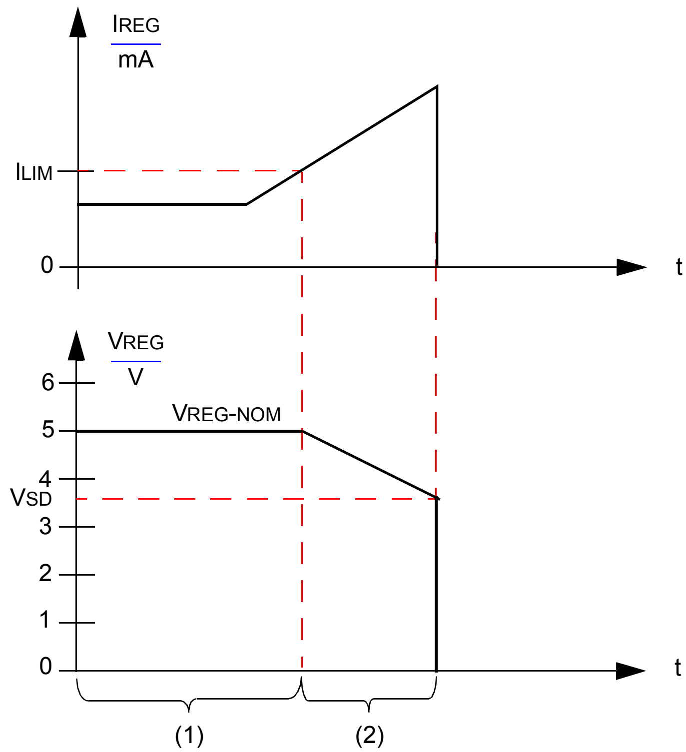
Note:	The regulator has an overload current limiting of approximately 100 mA. If VREG is lower than 2.5V, the VREG will turn off.

FIGURE 1-10: VOLTAGE REGULATOR OUTPUT ON POR



Note 1: Start-up, VBB < VON, regulator off.
2: VBB > VON, regulator on.
3: VBB ≤ Minimum VBB to maintain regulation.
4: VBB < VOFF, regulator will turn off.

FIGURE 1-11: VOLTAGE REGULATOR OUTPUT ON OVERCURRENT SITUATION



Note 1: IREG less than ILIM, regulator on.

2: After IREG exceeds ILIM, the voltage regulator output will be reduced until VSD is reached.

1.7 ICSP™ Considerations

The following should be considered when the MCP2021/2/1P/2P is connected to pins supporting in-circuit programming:

- Power used for programming the microcontroller can be supplied from the programmer or from the MCP2021/2/1P/2P.
- The voltage on VREG should not exceed the maximum output voltage of VREG.

NOTES:

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{IN} DC Voltage on R_{XD} and T_{XD} .... -0.3 to V_{REG}+0.3V

V_{IN} DC Voltage on $\overline{\text{FAULT}}$ and $\overline{\text{RESET}}$ .... -0.3 to +5.5V

V_{IN} DC Voltage on CS/LWAKE .... -0.3 to +43V

V_{BB} Battery Voltage, non-operating (LIN bus recessive, no regulator load, t < 60s) .... -0.3 to +43V

V_{BB} Battery Voltage, transient ISO 7637 Test 1 .... -200V

V_{BB} Battery Voltage, transient ISO 7637 Test 2a .... +150V

V_{BB} Battery Voltage, transient ISO 7637 Test 3a .... -300V

V_{BB} Battery Voltage, transient ISO 7637 Test 3b .... +200V

V_{BB} Battery Voltage, continuous .... -0.3 to +30V

V_{LBUS} Bus Voltage, continuous .... -18 to +30V

V_{LBUS} Bus Voltage, transient (**Note 1**) .... -27 to +43V

I_{LBUS} Bus Short Circuit Current Limit .... 200 mA

ESD protection on LIN, V_{BB} (IEC 61000-4-2, 330 Ohm, 150 pF) (**Note 3**) .... minimum ±9 kV

ESD protection on LIN, V_{BB} (Charge Device Model) (**Note 2**) .... ±1500V

ESD protection on LIN, VBB (Human Body Model, 1 kOhm, 100 pF) (**Note 4**) .... ±8 kV

ESD protection on LIN, V_{BB} (Machine Model) (**Note 2**) .... ±800V

ESD protection on all other pins (Human Body Model) (**Note 2**) .... > 4 kV

Maximum Junction Temperature .... 150°C

Storage Temperature .... -55 to +150°C

Note 1: ISO 7637/1 load dump compliant (t < 500 ms).

2: According to JESD22-A114-B.

3: According to IBEE, without bus filter.

4: Limited by Test Equipment.

† **NOTICE**: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2.2 DC Specifications

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C C_{REG} = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power						
V_{BB} Quiescent Operating Current	I_{BBQ}		115	210	µA	I_{OUT} = 0 mA, L_{BUS} recessive
		—	120	215	µA	V_{OUT} = 3.3V
V_{BB} Transmitter-Off Current	I_{BBTO}	—	90	190	µA	With V_{REG} on, transmitter off, receiver on, $\overline{FAULT}/TX_E$ = V_{IL}, CS = V_{IH}
		—	95	210	µA	V_{OUT} = 3.3V
V_{BB} Power-Down Current	I_{BBPD}	—	16	26	µA	With V_{REG} powered-off, receiver on and transmitter off, $\overline{FAULT}/TX_E$ = V_{IH}, TX_D = V_{IH}, CS = V_{IL})
V_{BB} Current with V_{SS} Floating	$I_{BBNOGND}$	-1	—	1	mA	V_{BB} = 12V, GND to V_{BB}, V_{LIN} = 0-18V
Microcontroller Interface						
High-Level Input Voltage (TX_D, $\overline{FAULT}/TX_E$)	V_{IH}	2.0 or (0.25V_{REG} + 0.8)	—	V_{REG} +0.3	V	
Low-Level Input Voltage (TX_D, $\overline{FAULT}/TX_E$)	V_{IL}	-0.3	—	0.15 V_{REG}	V	
High-Level Input Current (TX_D, $\overline{FAULT}/TX_E$)	I_{IH}	-2.5	—	—	µA	Input voltage = 0.8*V_{REG}
Low-Level Input Current (TX_D, $\overline{FAULT}/TX_E$)	I_{IL}	-10	—	—	µA	Input voltage = 0.2*V_{REG}
Pull-up Current on Input (TX_D)	I_{PUTXD}	-3.0	—	—	µA	~800 kΩ internal pull-up to V_{REG} @ V_{IH} = 0.7*V_{REG}
High-Level Input Voltage (CS/LWAKE)	V_{IH}	0.7 V_{REG}	—	V_{BB}	V	Through a current-limiting resistor
Low-Level Input Voltage (CS/LWAKE)	V_{IL}	-0.3	—	0.3V_{REG}	V	
High-Level Input Current (CS/LWAKE)	I_{IH}	—	—	7.0	µA	Input voltage = 0.8*V_{REG}
Low-Level Input Current (CS/LWAKE)	I_{IL}	—	—	3.0	µA	Input voltage = 0.2*V_{REG}
Pull-down Current on Input (CS/LWAKE)	I_{PDCS}	—	—	6.0	µA	~1.3 MΩ internal pull-down to V_{SS} @ V_{IH} = 3.5V

Note 1: Internal current limited. 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).

2: Characterized, not 100% tested.

3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.2 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for: VBB = 6.0V to 18.0V TA = -40°C to +125°C CREG = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Bus Interface						
High-Level Input Voltage	VIH(LBUS)	0.6 VBB	—	18	V	Recessive state
Low-Level Input Voltage	VIL(LBUS)	-8	—	0.4 VBB	V	Dominant state
Input Hysteresis	VHYS	—	—	0.175 VBB	V	VIH (LBUS) - VIL(LBUS)
Low-Level Output Current	IOL(LBUS)	40	—	200	mA	Output voltage = 0.1 VBB, VBB = 12V
Pull-up Current on Input	IPU(LBUS)	5	—	180	µA	~30 kΩ internal pull-up @ VIH (LBUS) = 0.7 VBB
Short Circuit Current Limit	ISC	50	—	200	mA	(**Note 1**)
High-Level Output Voltage	VOH(LBUS)	0.8 VBB	—	VBB	V	VOH (LBUS) must be at least 0.8 VBB
Low-Level Output Voltage	VOLLO (LBUS)	—	—	0.2 VBB	V	
Input Leakage Current (at the receiver during dominant bus level)	IBUS_PAS_DOM	-1	—	—	mA	Driver off, VBUS = 0V, VBAT = 12V
Leakage Current (disconnected from ground)	IBUS_NO_GND	-1	—	+1	mA	GNDDEVICE = VBAT, 0V < VBUS < 18V, VBAT = 12V
Leakage Current (disconnected from VBAT)	IBUS	—	—	10	µA	VBAT = GND, 0 < VBUS < 18V, TA = -40°C to +85°C (**Note 3**)
				50	µA	TA = +85°C to +125°C
Receiver Center Voltage	VBUS_CNT	0.475 VBB	0.5 VBB	0.525 VBB	V	VBUS_CNT = (VIL (LBUS) + VIH (LBUS))/2
Slave Termination	Rslave	20	30	47	kΩ	
Voltage Regulator – 5.0V						
Output Voltage	VOUT	4.85	5.00	5.15	V	0 mA < IOUT < 50 mA,
Load Regulation	ΔVOUT2	—	10	50	mV	5 mA < IOUT < 50 mA refer to **Section 1.6 "Internal Voltage Regulator"**
Quiescent Current	IVRQ	—	—	25	µA	IOUT = 0 mA, (**Note 2**)
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 VPP @10-20 kHz CLOAD = 10 µf, ILOAD = 50 mA

Note 1: Internal current limited. 2.0 ms maximum recovery time (RLBUS = 0Ω, TX = 0.4 VREG, VLBUS = VBB).

2: Characterized, not 100% tested.

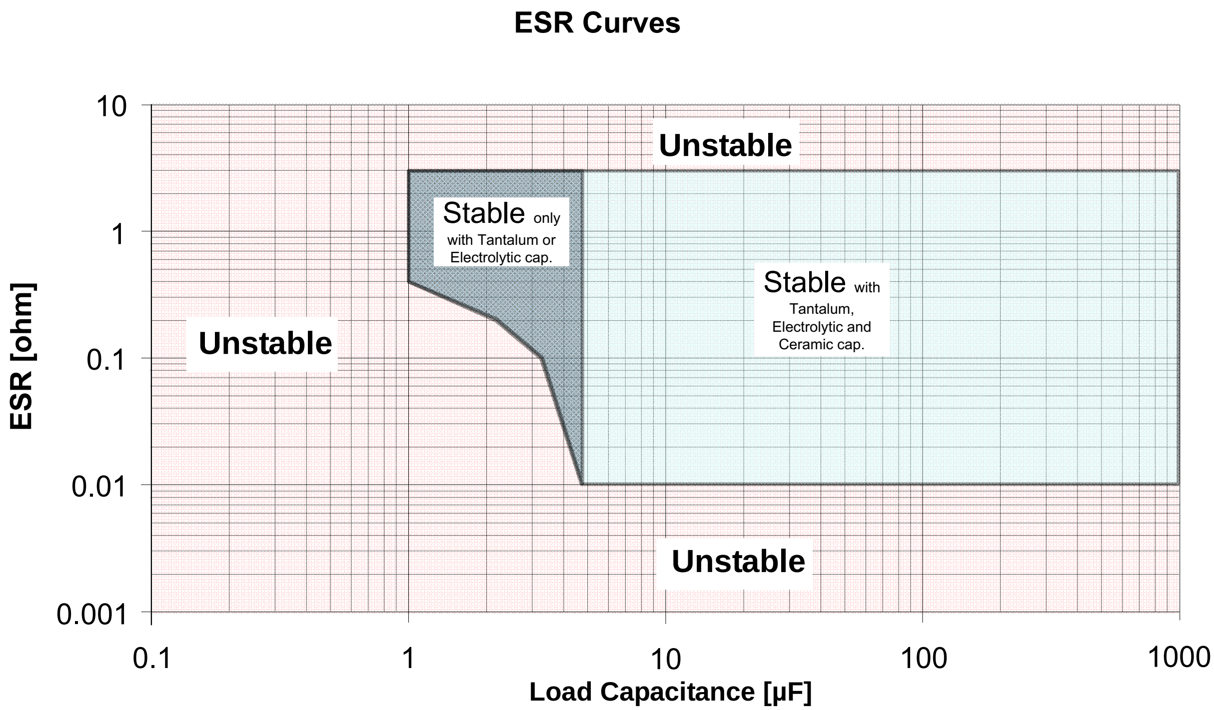
3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.2 DC Specifications (Continued)

DC Specifications	Electrical Characteristics: Unless otherwise indicated, all limits are specified for: V_{BB} = 6.0V to 18.0V T_A = -40°C to +125°C C_{REG} = 10 µF					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Noise Voltage	eN	—	—	100	µVRMS	10 Hz – 40 MHz CFILTER = 10 µf, CBP = 0.1 µf, CLOAD 10 µf, ILOAD = 50 mA
Shutdown Voltage	VSD	3.5	—	4.0	V	See Figure 1-11 (**Note 2**)
Input Voltage to Maintain Regulation	VBB	6.0	—	18.0	V	
Input Voltage to Turn Off Output	VOFF	4.0	—	4.5	V	
Input Voltage to Turn On Output	VON	5.5	—	6.0	V	
Voltage Regulator – 3.3V						
Output Voltage	VOUT	3.20	3.30	3.40	V	0 mA < IOUT < 50 mA
Line Regulation	ΔVOUT1	—	10	50	mV	IOUT = 1 mA, 6.0V < VBB < 18V
Load Regulation	ΔVOUT2	—	10	50	mV	5 mA < IOUT < 50 mA Refer to **Section 1.6 "Internal Voltage Regulator"**
Quiescent Current	IVRQ	—	—	25	µA	IOUT = 0 mA, (**Note 2**)
Power Supply Ripple Reject	PSRR	—	—	50	dB	1 VPP @10-20 kHz CLOAD = 10 µf, ILOAD = 50 mA
Output Noise Voltage	eN	—	—	100	µVRMS /√Hz	10 Hz – 40 MHz CFILTER = 10 µf, CBP = 0.1 µf CLOAD = 10 µf, ILOAD = 50 mA
Shutdown Voltage	VSD	2.5	—	2.7	V	See Figure 1-11 (**Note 2**)
Input Voltage to Maintain Regulation	VBB	6.0	—	18.0	V	
Input Voltage to Turn Off Output	VOFF	4.0	—	4.5	V	
Input Voltage to Turn On Output	VON	5.5	—	6.0	V	

Note 1: Internal current limited. 2.0 ms maximum recovery time (RLBUS = 0Ω, TX = 0.4 VREG, VLBUS = VBB).
2: Characterized, not 100% tested.
3: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

FIGURE 2-1: ESR CURVES FOR LOAD CAPACITOR SELECTION



Note: The graph shows the minimum required capacitance after derating due to tolerance, temperature and voltage.

2.3 AC Specification

AC CHARACTERISTICS	V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Bus Interface – Constant Slope Time Parameters						
Slope rising and falling edges	t_{SLOPE}	3.5	—	22.5	µs	7.3V <= V_{BB} <= 18V
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	4.0	µs	$t_{TRANSPD}$ = max ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	µs	t_{RECPD} = max (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver rising edge w.r.t. falling edge	t_{RECSYM}	-2.0	—	2.0	µs	t_{RECSYM} = max (t_{RECPDF} - t_{RECPDR})
Symmetry of Propagation Delay of Transmitter rising edge w.r.t. falling edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF}$ - $t_{TRANSPDR}$)
Time to sample of $\overline{FAULT}$/T_{XE} for bus conflict reporting	t_{FAULT}	—	—	32.5	µs	t_{FAULT} = max ($t_{TRANSPD}$ + t_{SLOPE} + t_{RECPD})
Duty Cycle 1 @20.0 kbit/sec		39.6	—	—	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω |10 nF; 500Ω $TH_{REC(MAX)}$ = 0.744 x V_{BB}, $TH_{DOM(MAX)}$ = 0.581 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 50 µs. D1 = $t_{BUS\_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 2 @20.0 kbit/sec		—	—	58.1	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω |10 nF; 500Ω $TH_{REC(MAX)}$ = 0.284 x V_{BB}, $TH_{DOM(MAX)}$ = 0.422 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 50 µs. D2 = $t_{BUS\_REC(MAX)}$ / 2 x t_{BIT})
Duty Cycle 3 @10.4 kbit/sec		41.7	—	—	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω |10 nF; 500Ω$TH_{REC(MAX)}$ = 0.778 x V_{BB}, $TH_{DOM(MAX)}$ = 0.616 x V_{BB}, V_{BB} =7.0V - 18V; t_{BIT} = 96 µs. D3 = $t_{BUS\_REC(MIN)}$ / 2 x t_{BIT})
Duty Cycle 4 @10.4 kbit/sec		—	—	59.0	%t_{BIT}	C_{BUS};R_{BUS} conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω |10 nF; 500Ω $TH_{REC(MAX)}$ = 0.251 x V_{BB}, $TH_{DOM(MAX)}$ = 0.389 x V_{BB}, V_{BB} =7.6V - 18V; t_{BIT} = 96 µs. D4 = $t_{BUS\_REC(MAX)}$ / 2 x t_{BIT})

Note 1: Time depends on external capacitance and load. Test condition: CREG=4.7 µF, no resistive load.
2: Characterized, not 100% tested.

2.3 AC Specification (Continued)

AC CHARACTERISTICS	V_{BB} = 6.0V to 18.0V; T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Voltage Regulator						
Bus Activity Debounce Time	t_{BDB}	5	10	20	µs	Bus debounce time
Bus Activity to Voltage Regulator Enabled	t_{BACTVE}	100	250	500	µs	After bus debounce time
Voltage Regulator Enabled to Ready	t_{VEVR}	—	—	1200	µs	**(Note 1)**
Chip Select to Operation Ready	t_{CSR}	—	—	500	µs	
Chip Select to Power-Down	t_{CSPD}	—	—	80	µs	**(Note 2)**
Short-Circuit to Shut-Down	$t_{SHUTDOWN}$	20	—	100	µs	
$\overline{\text{RESET}}$ Timing						
V_{REG} OK Detect to $\overline{\text{RESET}}$ Inactive	t_{RPU}	—	—	10.0	µs	
V_{REG} OK Detect to $\overline{\text{RESET}}$ Active	t_{RPD}	—	—	10.0	µs	

Note 1: Time depends on external capacitance and load. Test condition: CREG=4.7 µF, no resistive load.
2: Characterized, not 100% tested.

2.4 Thermal Specifications (Note 1)

THERMAL CHARACTERISTICS					
Parameter	**Symbol**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Recovery Temperature	$\theta_{RECOVERY}$	+140	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	+150	—	°C	
Short Circuit Recovery Time	t_{THERM}	1.5	5.0	ms	
Thermal Package Resistances					
Thermal Resistance, 4x4 8L-DFN	θ_{JA}	48	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	149.5	—	°C/W	
Thermal Resistance, 14L-PDIP	θ_{JA}	70	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	90.8	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	100	—	°C/W	

Note 1: The maximum power dissipation is a function of T_{JMAX}, θ_{JA} and ambient temperature T_A. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A)\ \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above 150°C and the MCP2021 will go into thermal shutdown.

2.5 Typical Performance Curves

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, VBB = 6.0V to 18.0V; TA = -40°C to +125°C.

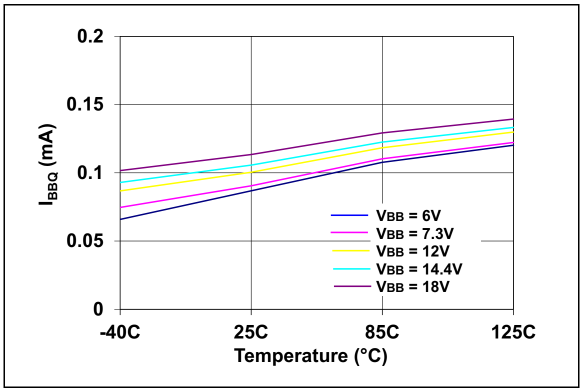


FIGURE 2-2: Typical I_{BBQ} vs. Temperature.

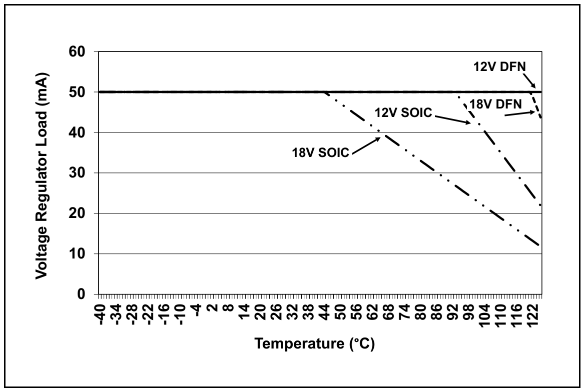


FIGURE 2-5: MCP2021-500 Safe Operating Range.

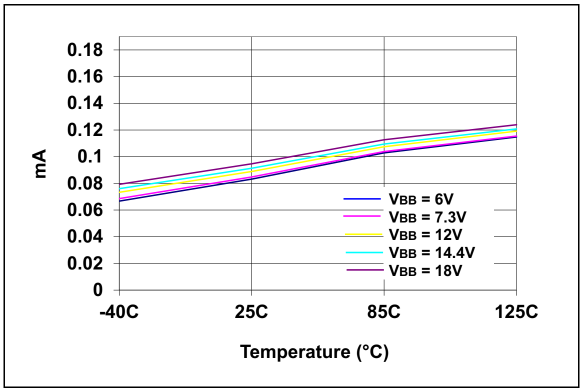


FIGURE 2-3: Typical I_{BBTO} vs Temperature.

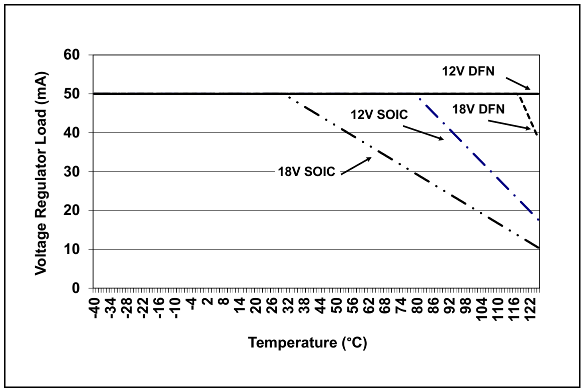


FIGURE 2-6: MCP2021-330 Safe Operating Range.

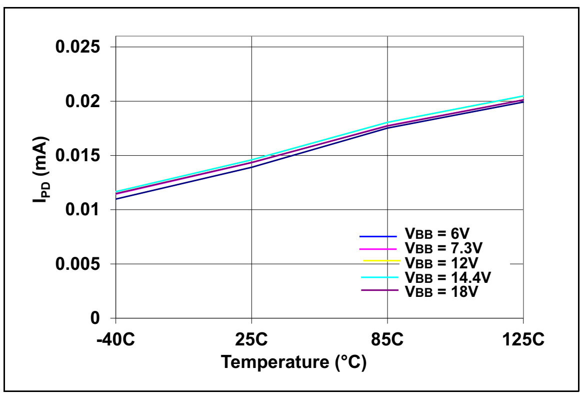


FIGURE 2-4: Typical I_{BBPD} vs. Temperature.

2.6 Timing Diagrams and Specifications

FIGURE 2-7: BUS TIMING DIAGRAM

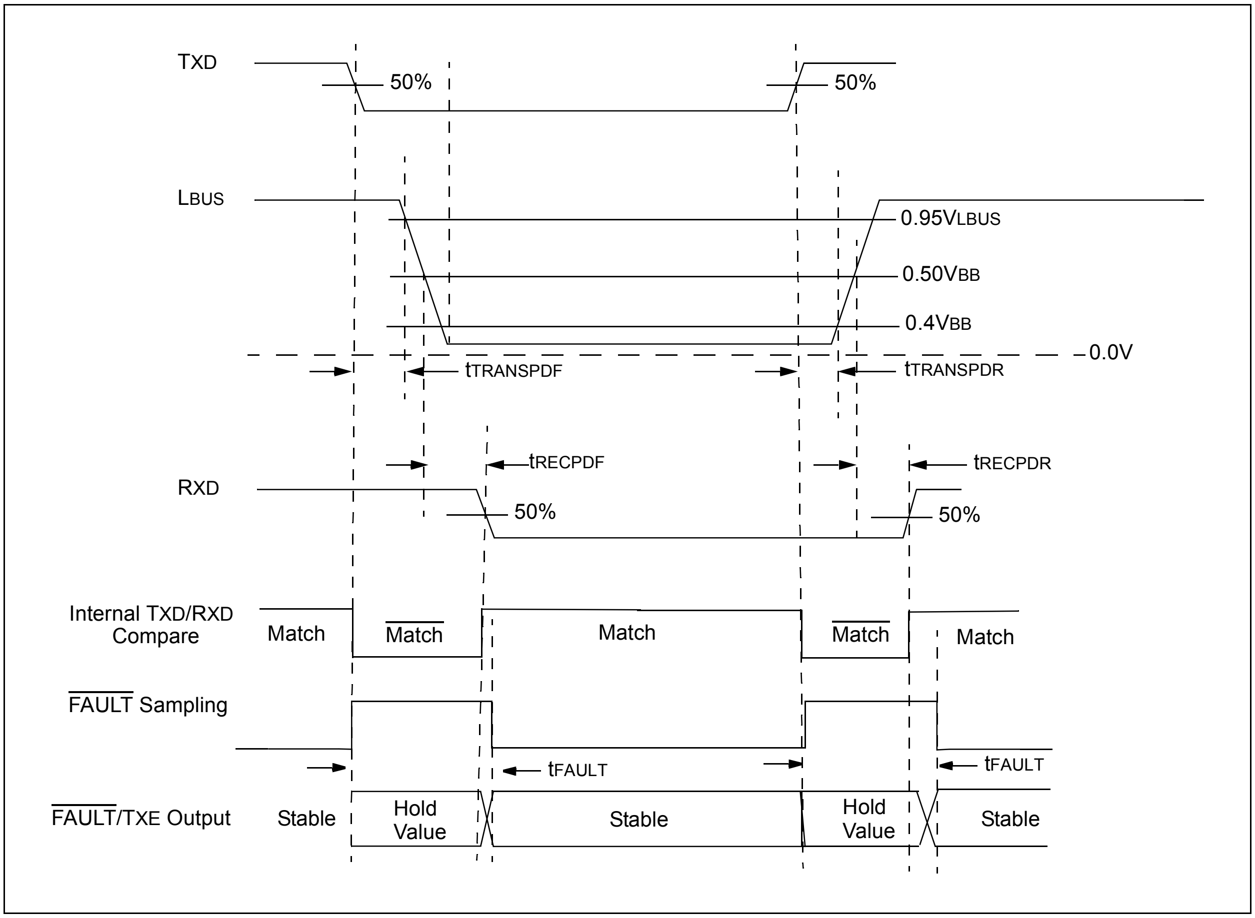


FIGURE 2-8: REGULATOR BUS WAKE TIMING DIAGRAM

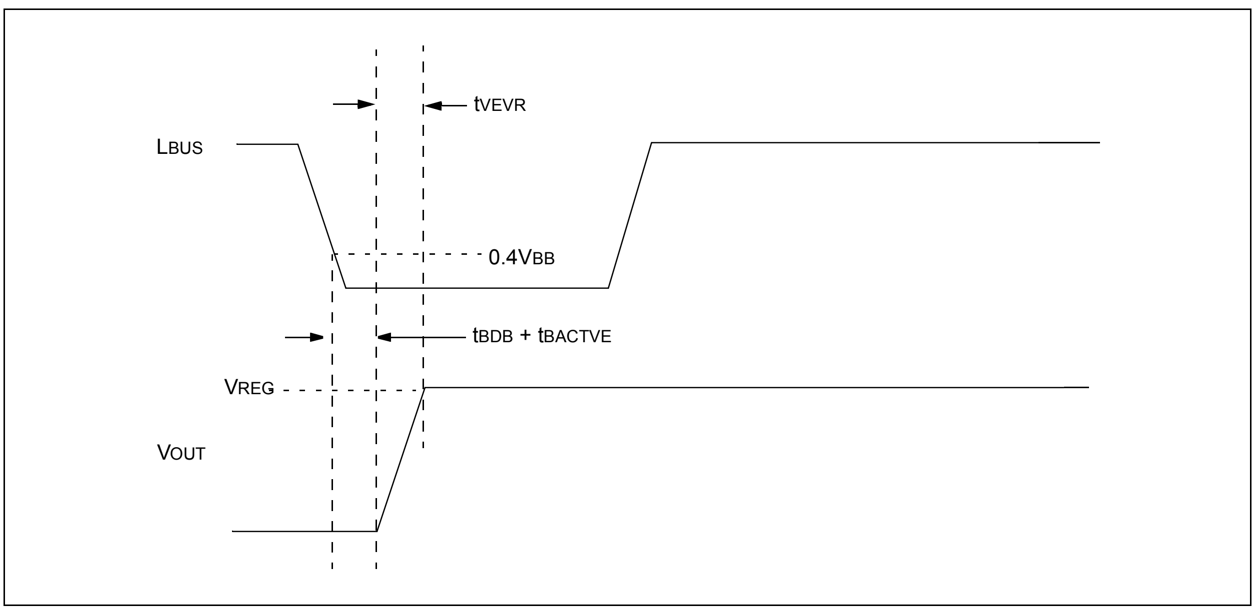


FIGURE 2-9: RESET TIMING DIAGRAM

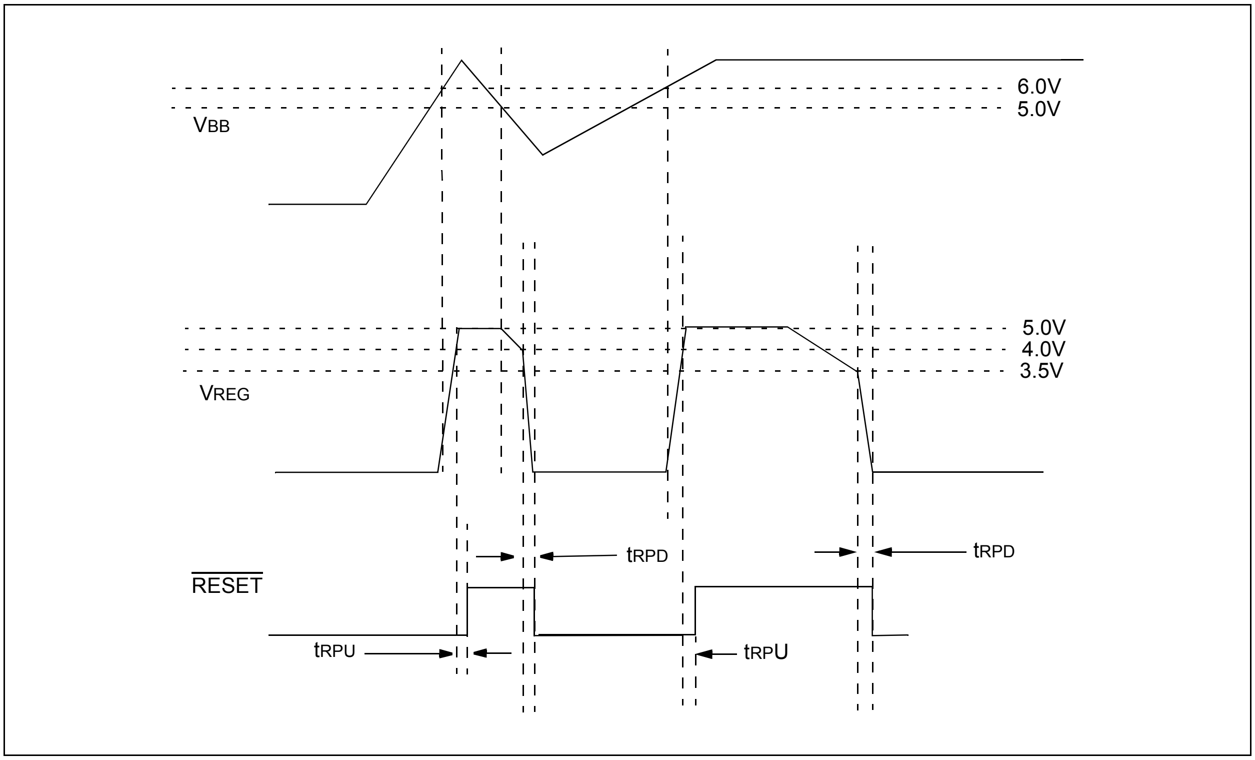
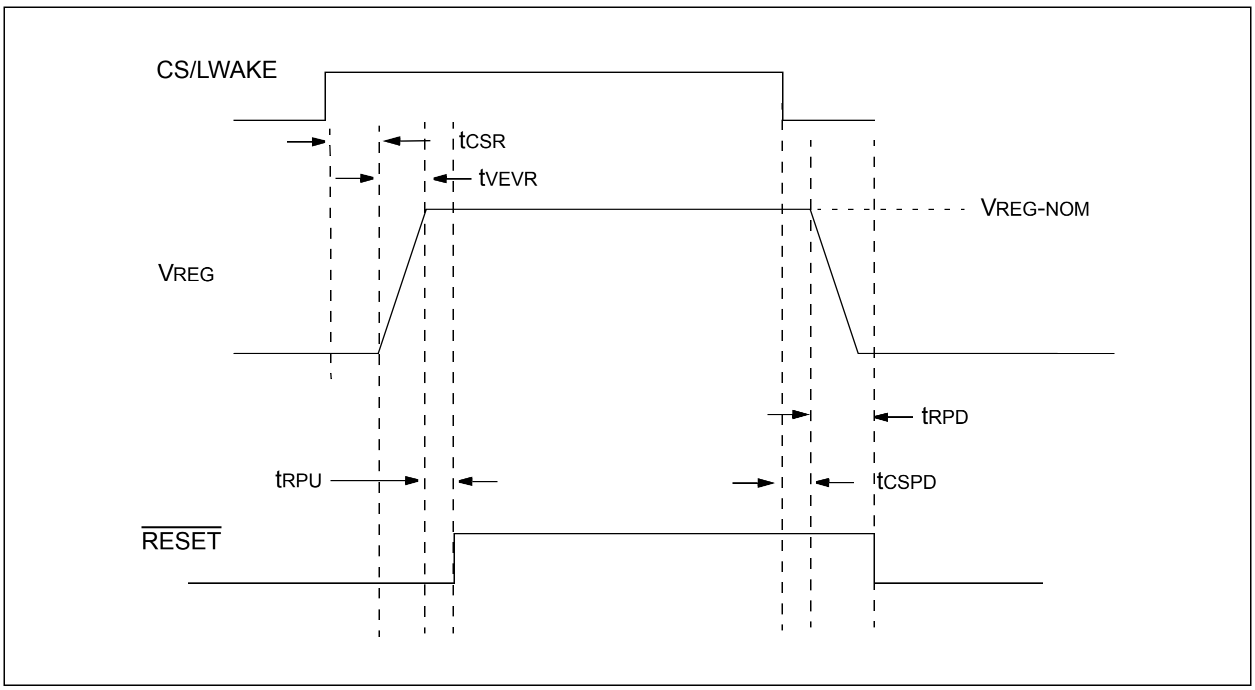


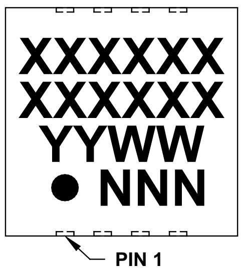
FIGURE 2-10: CS/LWAKE TO RESET TIMING DIAGRAM



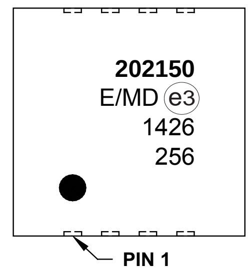
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

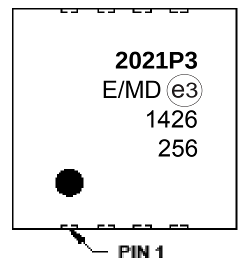
8-Lead DFN (4x4x0.9 mm) **(MCP2021, MCP2021P)**



Example

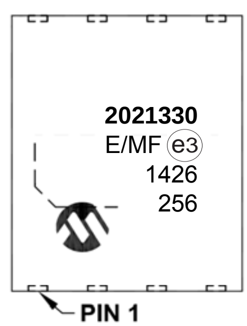


OR



8-Lead DFN-S (6x5x0.9 mm) **(MCP2021)**

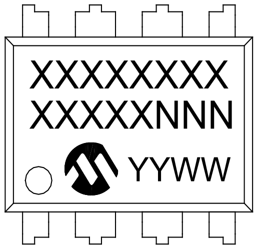
Example



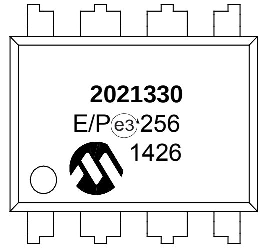
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

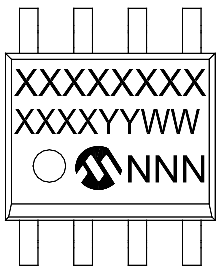
8-Lead PDIP (150 mil) **(MCP2021)**



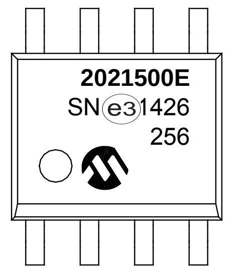
Example



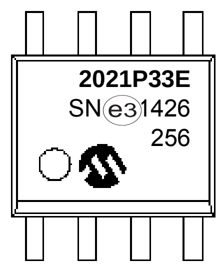
8-Lead SOIC (150 mil) **(MCP2021, MCP2021P)**



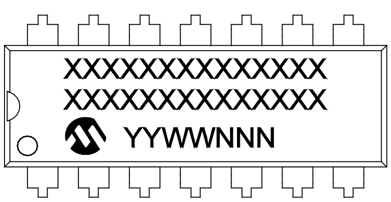
Example



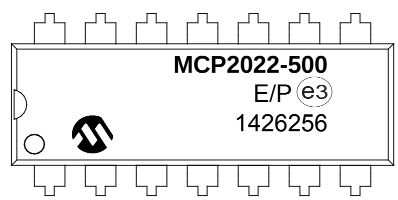
OR



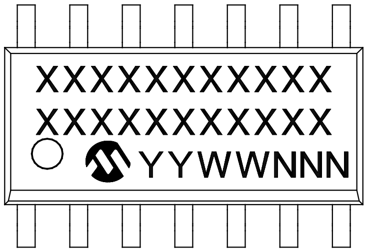
14-Lead PDIP (300 mil) **(MCP2022)**



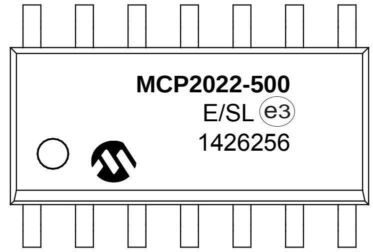
Example



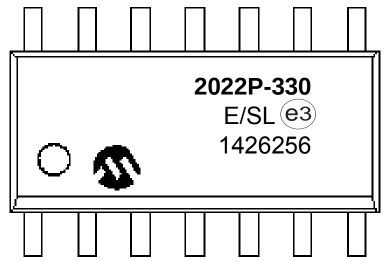
14-Lead SOIC (150 mil) **(MCP2022, MCP2022P)**



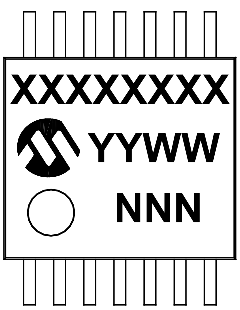
Example



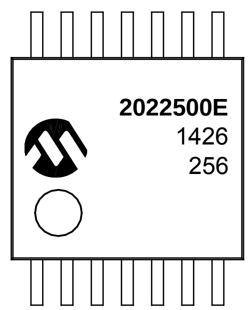
OR



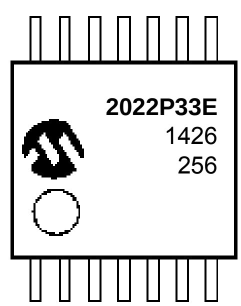
14-Lead TSSOP (4.4 mm) **(MCP2022, MCP2022P)**



Example

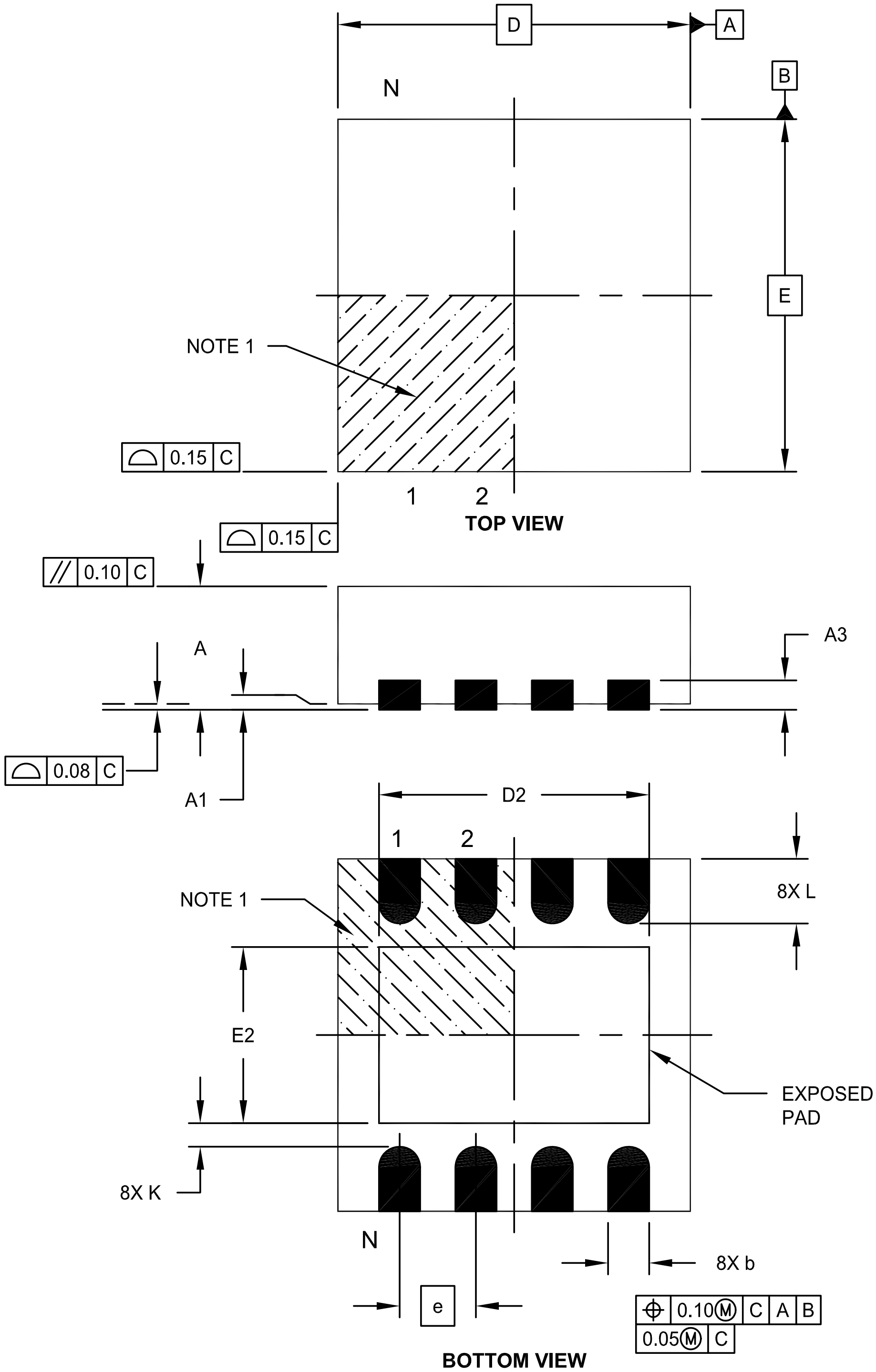


OR



8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

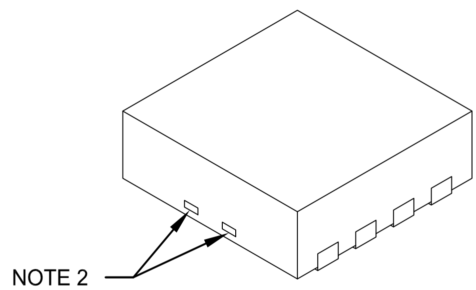
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-131E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.80 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	4.00 BSC		
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Width	E	4.00 BSC		
Exposed Pad Length	D2	3.40	3.50	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

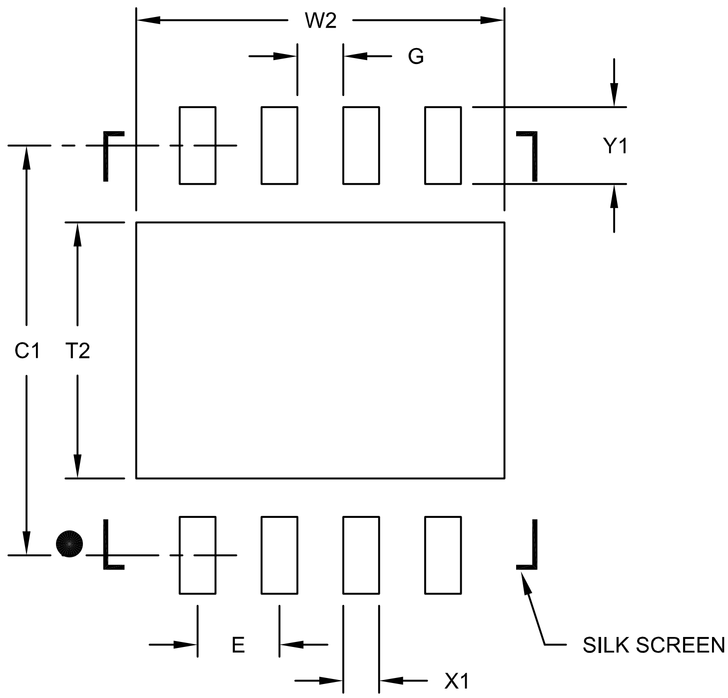
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:

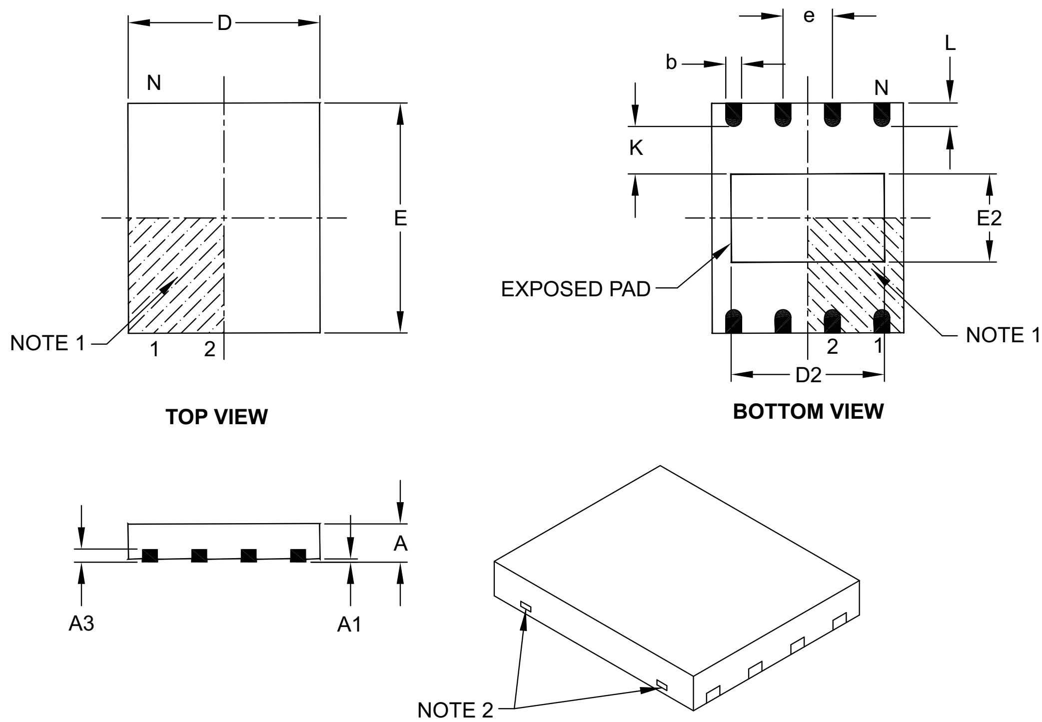
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		5.00 BSC	
Overall Width	E		6.00 BSC	
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

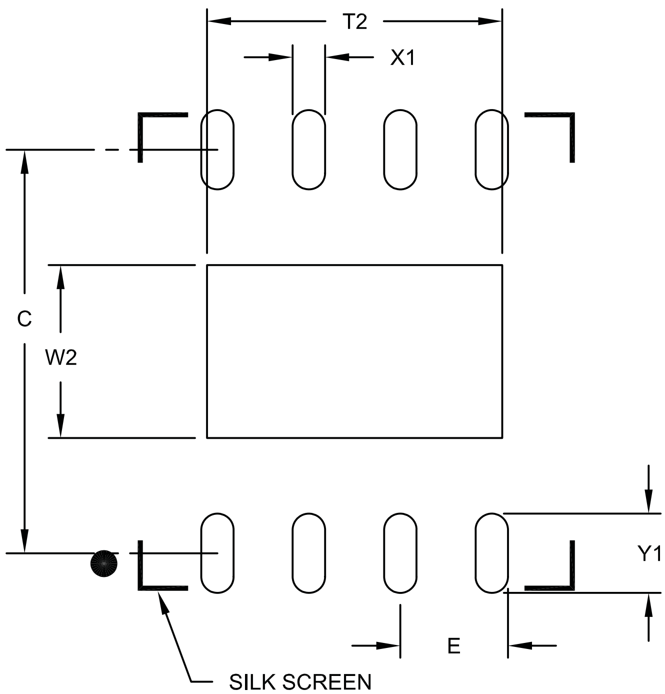
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122B

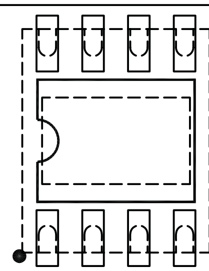
8-Lead Plastic Dual Flat, No Lead Package (MF) - 6x5 mm Body [DFN-S]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

NOTE: THIS PACKAGE MAY ALSO BE USED WITH THE 8L SOIC (3.90 mm) LAND PATTERN



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Optional Center Pad Width	W2			2.40
Optional Center Pad Length	T2			4.10
Contact Pad Spacing	C		5.60	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.10

Notes:

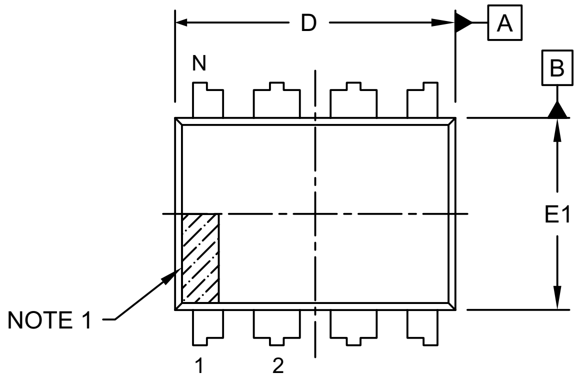
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

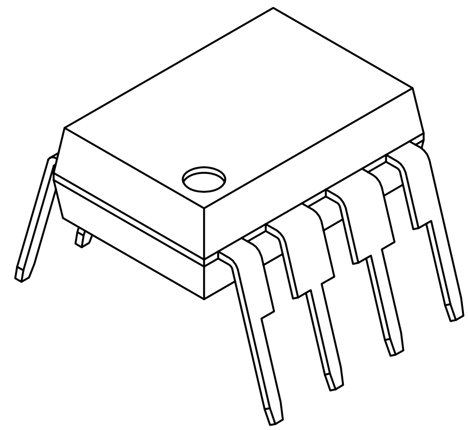
Microchip Technology Drawing No. C04-2122A

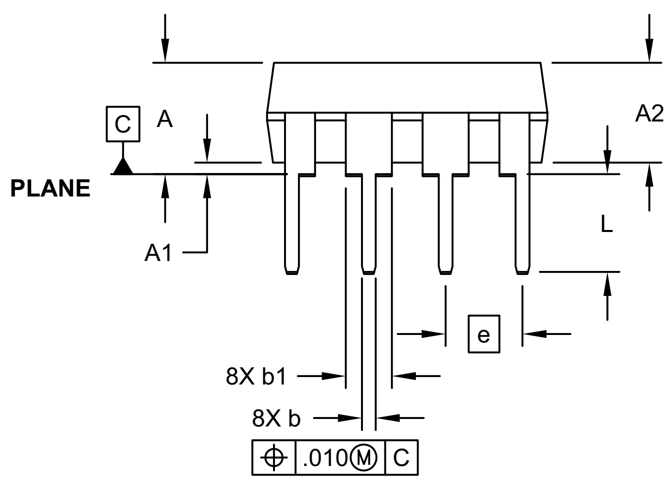
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

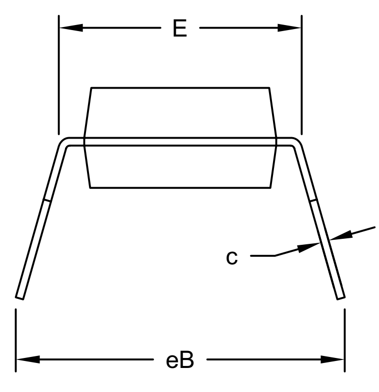


TOP VIEW





SIDE VIEW

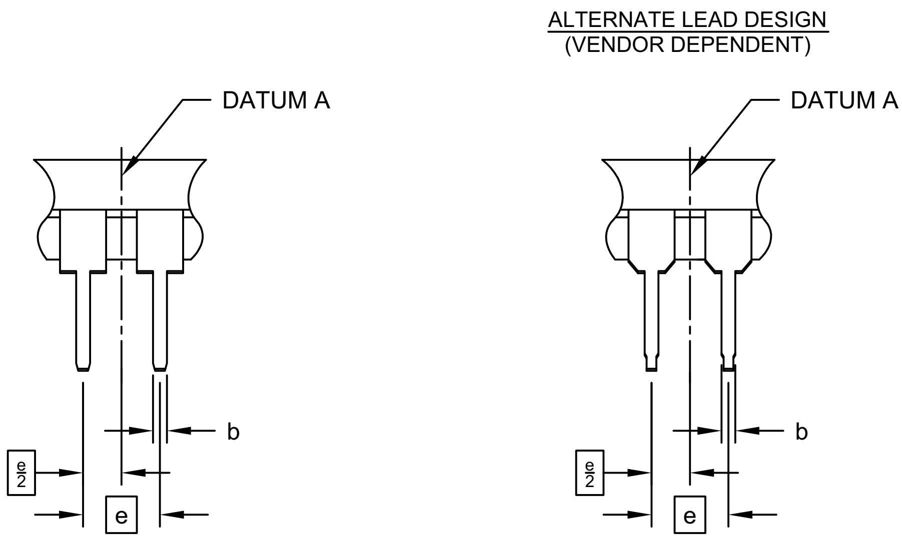


END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

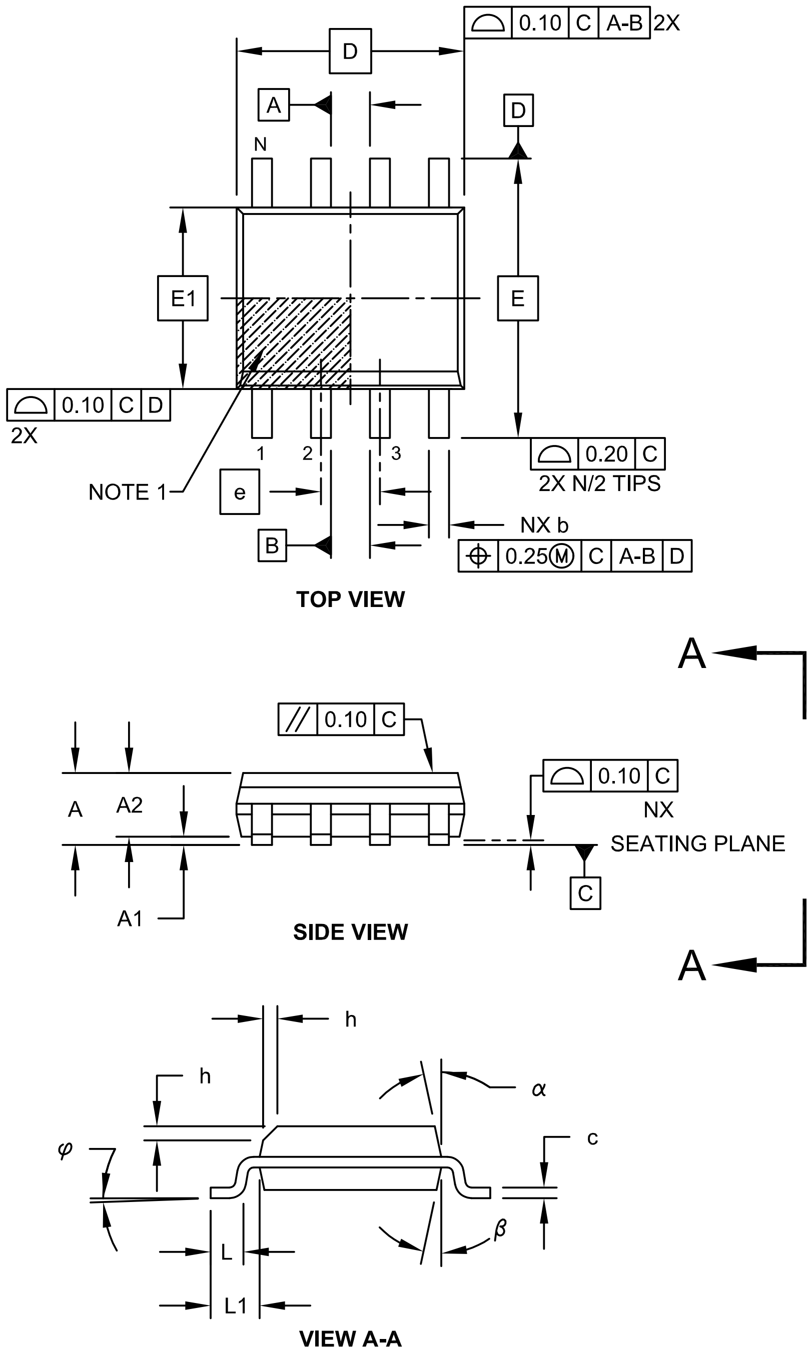
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

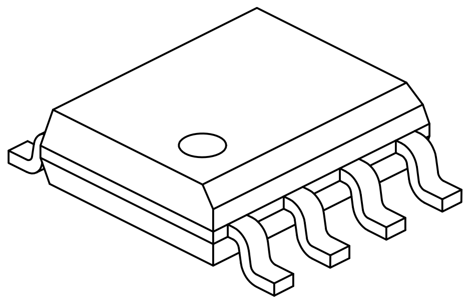
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

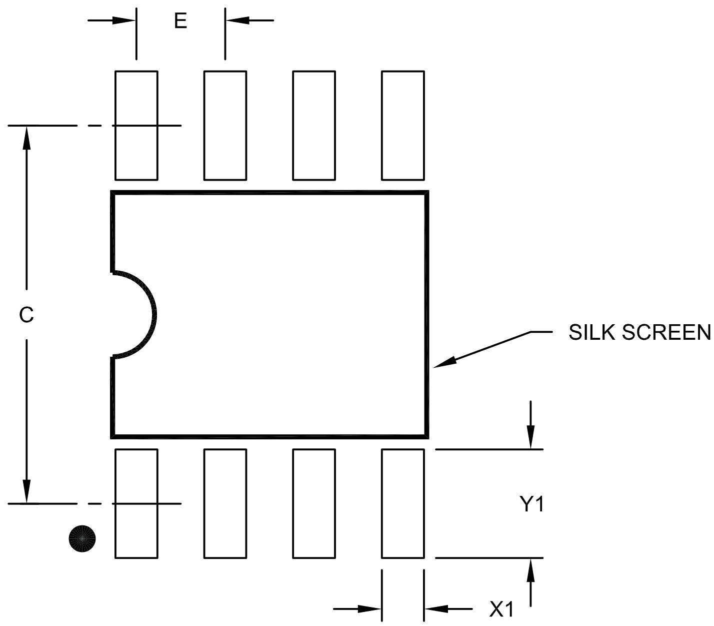
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

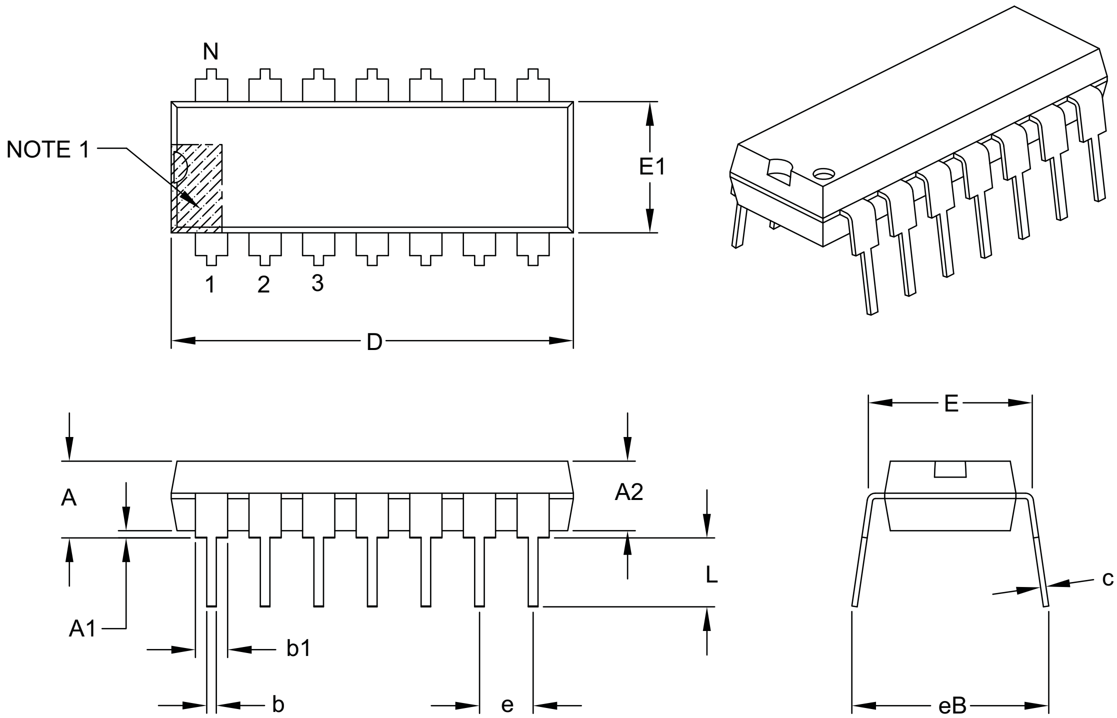
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

14-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.735	.750	.775
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

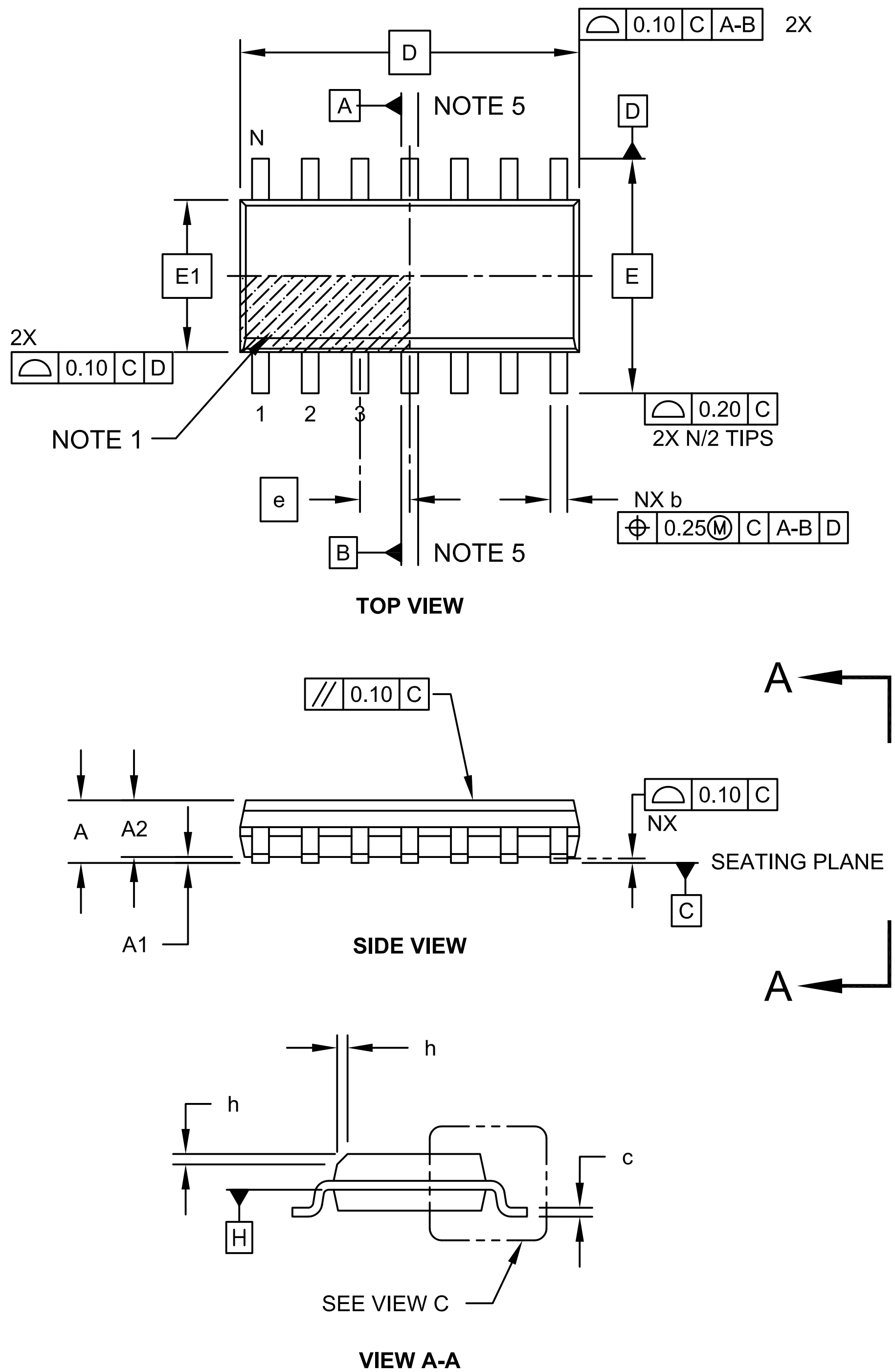
Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-005B

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

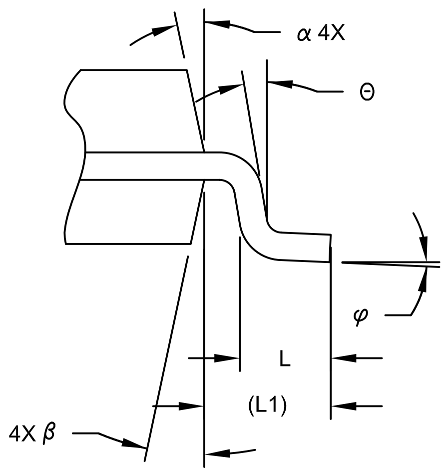
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



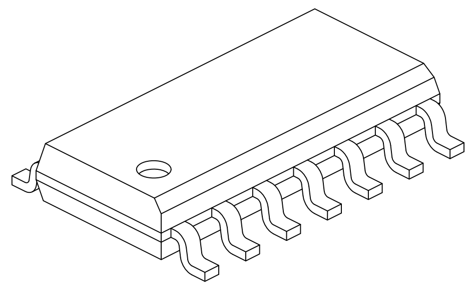
Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C



	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

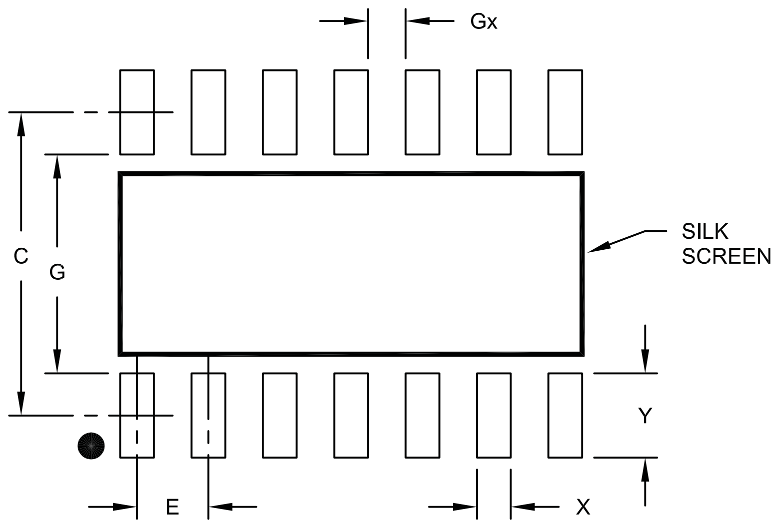
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

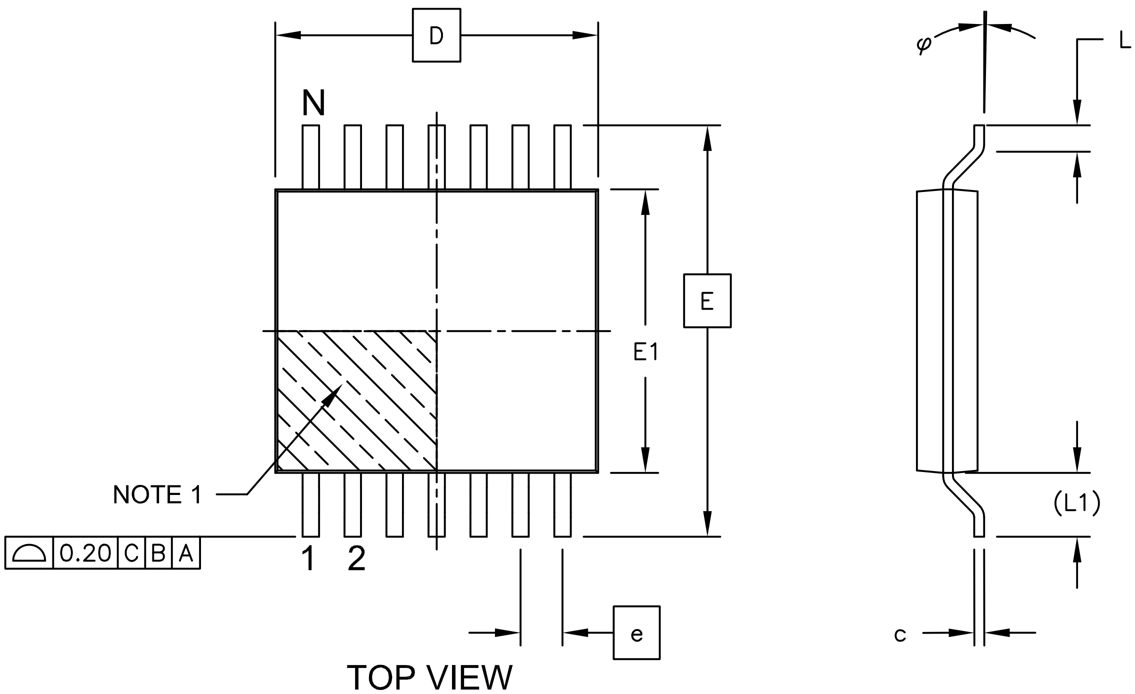
1. Dimensioning and tolerancing per ASME Y14.5M

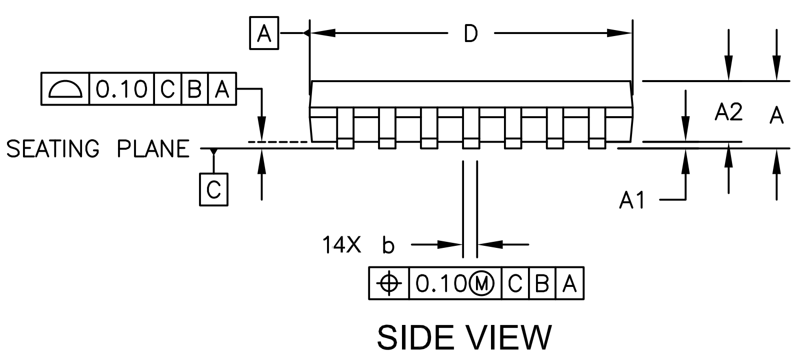
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

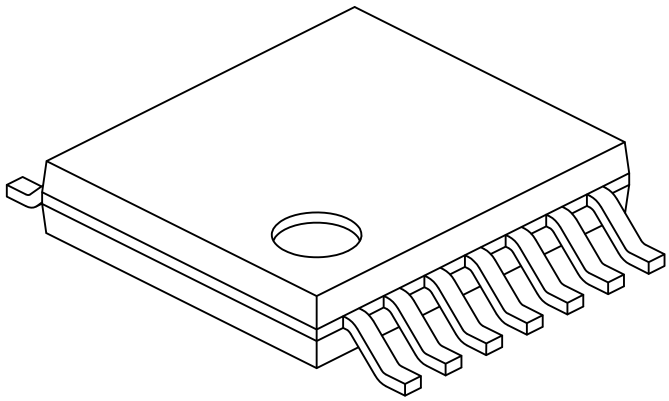




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

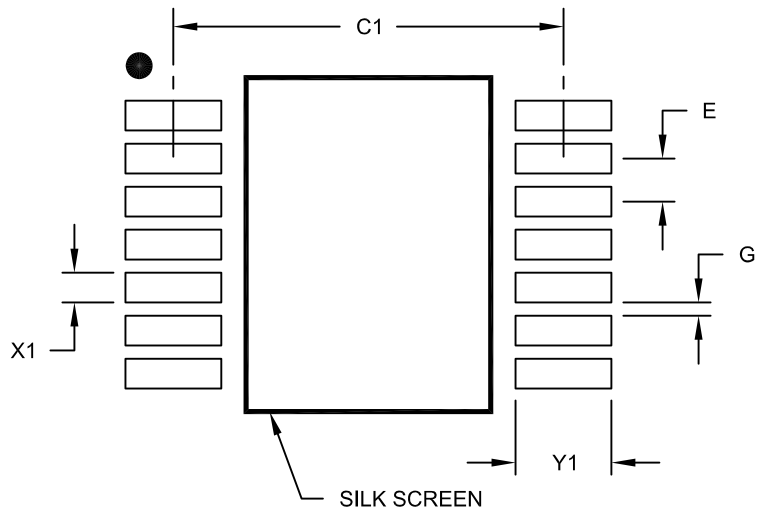
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X14)	X1			0.45
Contact Pad Length (X14)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

APPENDIX A: REVISION HISTORY

Revision H (July 2014)

The following is the list of modifications:

1. Updated **Table 1-1**.
2. Updated **Section 1.4, Pin Descriptions** and **Section 1.6.1 “5.0V Regulator”**.
3. Updated **Figures 1-6** and **1-7.**
4. Updated **Figures 1-10** and **1-11.**
5. Added **Section 2.5, Typical Performance Curves**.
6. Updated **Section 3.0, Packaging Information**.
7. Updated the **Product Identification System** section.
8. Minor typographical changes.

Revision G (July 2013)

The following has been modified:

1. Added Note 2 in **Section 2.3 “AC Specification”**.
2. Added pull up to nFAULT/TXE pin in **Section 1.4 “Pin Descriptions”** and **Section 1.5 “Typical Applications”**.

Revision F (January 2012)

The following has been modified:

1. Added the MCP2021P and MCP2022P options and related information throughout the document.

Revision E (February 2009)

The following is the list of modifications:

1. Added Example 1-7 and Example 1-8.
2. Updated **Section 1.4.10 “RESET”**.
3. Updated **Section 1.7 “ICSP™ Considerations”**.
4. Updated **Section 2.1 “Absolute Maximum Ratings†”**.
5. Updated **Section 2.2 “DC Specifications”** and **Section 2.3 “AC Specification”**.
6. Added **Figure 2-1** in **Section 2.0 “Electrical Characteristics”**
7. Updated the Product Identification System section.

Revision D (July 2008)

The following is the list of modifications:

1. Updated ESD specs under ‘Absolute DC’.
2. Updated notes in Example 1-1.
3. Updated Package Outline Drawings.

Revision C (April 2008)

The following is the list of modifications:

1. Added LIN2.1 and J2602 compliance statement to Features section.
2. Added recommended RC network for CS/LWAKE in Example 1-1.
3. Updated **2.1 “Absolute Maximum Ratings†”** to reflect current test results.
4. Updated **2.2 “DC Specifications”** and **2.3 “AC Specification”** 2.3 AC Specifications to reflect current production device.
5. Added 8-Lead SOIC Landing Pattern Outline drawing.

Revision B (August 2007)

The following is the list of modifications:

1. Modified Block Diagram on page 2.
2. **Section 1.3.5 “Transmitter-OFF Mode”**: Deleted text in 1st paragraph.
3. **Example 1-6**: Removed +5V notation.
4. **Section 1.4 “Pin Descriptions”**: Removed 10-pin DFN, MSOP column from table.
5. **Section 1.4.9 “Fault/Txe”**: Deleted text from 2nd paragraph.
6. **Section 3.0 “Packaging Information”**: Added 8-lead 4x4 and 6x5 DFN and 14-lead TSSOP packages. Updated package outline drawings and added drawings for 8-lead DFN and 14-lead TSSOP drawings.

Revision A (November 2005)

Original Release of this Document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	X	/XX
Device	Voltage	Temperature Range	Package

Device:

- MCP2021: LIN Transceiver with Voltage Regulator; wakes up on dominant level of LIN bus.
- MCP2021T: LIN Transceiver with Voltage Regulator; wakes up on dominant level of LIN bus. (Tape and Reel) (SOIC only)
- MCP2022: LIN Transceiver with Voltage Regulator, and RESET pin; wakes up on dominant level of LIN bus.
- MCP2022T: LIN Transceiver with Voltage Regulator, and RESET pin; wakes up on dominant level of LIN bus. (Tape and Reel) (SOIC only)
- MCP2021P: LIN Transceiver with Voltage Regulator; wakes up at a falling edge of LIN bus level.
- MCP2021PT: LIN Transceiver with Voltage Regulator; wakes up at a falling edge of LIN bus level (Tape and Reel) (SOIC only)
- MCP2022P: LIN Transceiver with Voltage Regulator, and RESET pin; wakes up at a falling edge of LIN bus level.
- MCP2022PT: LIN Transceiver with Voltage Regulator, and RESET pin; wakes up at a falling edge of LIN bus level. (Tape and Reel) (SOIC only)

Voltage:

- 330 = 3.3V
- 500 = 5.0V

Temperature Range:

- E = -40°C to +125°C (Extended)

Package:

- MD = 8-Lead Plastic Dual Flat, No Lead – 4x4x0.9 mm Body (DFN)
- MF = 8-Lead Plastic Dual Flat, No Lead – 6x5 mm Body (DFN-S)
- P = 14-Lead Plastic Dual In Line – 300 mil Body (PDIP)
- SN = 8-Lead Plastic Small Outline – Narrow, 3.90 mm Body (SOIC)
- SL = 14-Lead Plastic Small Outline – Narrow, 3.90 mm Body (SOIC)
- ST = 14-Lead Plastic Thin Shrink Small Outline – Narrow, 4.4 mm (TSSOP)

Examples:

a) MCP2021-500E/MD: 5.0V, Extended Temperature, 8L-DFN package.
b) MCP2021T-500E/MD: Tape and Reel, 5.0V, Extended Temperature, 8L-DFN package.
c) MCP2021-500E/MF: 5.0V, Extended Temperature, 8L-DFN-S package.
d) MCP2021-330E/P: 3.3V, Extended Temperature, 8L-PDIP package.
e) MCP2021-500E/P: 5.0V, Extended Temperature, 8L-PDIP package.
f) MCP2021-330E/SN: 3.3V, Extended Temperature, 8L-SOIC package
g) MCP2021T-330E/SN: Tape and Reel, 3.3V, Extended Temperature, 8L-SOIC package.
h) MCP2021-500E/SN: 5.0V, Extended Temperature, 8L-SOIC package.
i) MCP2021T-500E/SN: Tape and Reel, 5.0V, Extended Temperature, 8L-SOIC package.

a) MCP2022-330E/P: 3.3V, Extended Temperature, 14L-PDIP package.
b) MCP2022-500E/P: 5.0V, Extended Temperature, 14L-PDIP package.
c) MCP2022-330E/SL: 3.3V, Extended Temperature, 14L-SOIC package.
d) MCP2022T-330E/SL: Tape and Reel, 3.3V, Extended Temperature, 14L-SOIC package.
e) MCP2022-500E/SL: 5.0V, Extended Temperature, 14L-SOIC package.
f) MCP2022T-500E/SL: Tape and Reel, 5.0V, Extended Temperature, 14L-SOIC package.
g) MCP2022T-500E/ST: Tape and Reel, 5.0V, Extended Temperature, 14L-TSSOP package.

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