19-2622; Rev 2; 6/09

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators



## General Description

The MAX1951/MAX1952 high-efficiency, DC-to-DC step-down switching regulators deliver up to 2A of output current. The devices operate from an input voltage range of 2.6V to 5.5V and provide an output voltage from 0.8V to $V_{IN}$, making the MAX1951/MAX1952 ideal for on-board postregulation applications. The MAX1951 total output error is less than 1% over load, line, and temperature.

The MAX1951/MAX1952 operate at a fixed frequency of 1MHz with an efficiency of up to 94%. The high operating frequency minimizes the size of external components. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improve design reliability.

The MAX1951 provides an adjustable output from 0.8V to $V_{IN}$, whereas the MAX1952 has a preset output of 1.8V. Both devices are available in a space-saving 8-pin SO package.

## Applications

ASIC/DSP/µP/FPGA Core and I/O Voltages

Set-Top Boxes

Cellular Base Stations

Networking and Telecommunications

## Features

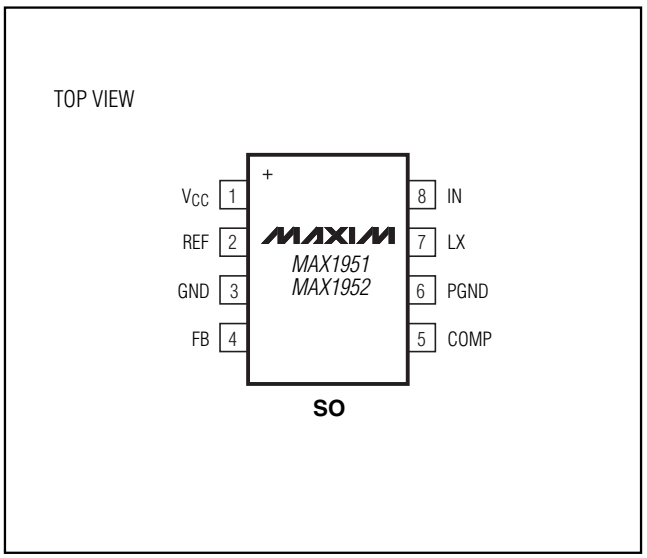
- **Compact 0.385in² Circuit Footprint**
- **10µF Ceramic Input and Output Capacitors, 2µH Inductor for 1.5A Output**
- **Efficiency Up to 94%**
- **1% Output Accuracy Over Load, Line, and Temperature (MAX1951, Up to 1.5A)**
- **Guaranteed 2A Output Current**
- **Operate from 2.6V to 5.5V Supply**
- **Adjustable Output from 0.8V to $V_{IN}$ (MAX1951)**
- **Preset Output of 1.8V (1.5% Accuracy) (MAX1952)**
- **Internal Digital Soft-Soft**
- **Short-Circuit and Thermal-Overload Protection**

## Ordering Information/ Selector Guide

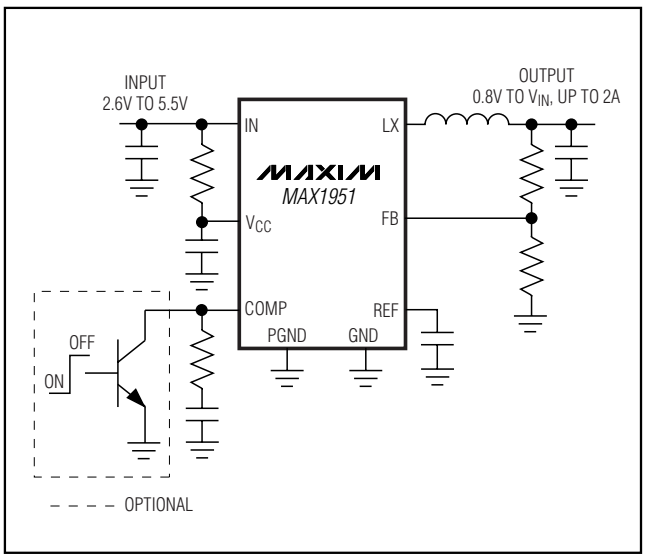
| PART | TEMP RANGE | PIN-PACKAGE | OUTPUT |
|---|---|---|---|
| **MAX1951**ESA+ | -40°C to +85°C | 8 SO | Adj 0.8V to $V_{IN}$ |
| **MAX1952**ESA+ | -40°C to +85°C | 8 SO | Fixed 1.8V |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

## Pin Configuration




## Typical Operating Circuit






**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.**

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

## ABSOLUTE MAXIMUM RATINGS

IN, $V_{CC}$ to GND .....-0.3V to +6V
COMP, FB, REF to GND .....-0.3V to ($V_{CC}$ + 0.3V)
LX to Current (Note 1).....±4.5A
PGND to GND .....Internally Connected
Continuous Power Dissipation ($T_A$ = +85°C)
8-Pin SO (derate 12.2mW/°C above +70°C).....976mW
Package Junction-to-Ambient
Thermal Resistance ($\theta_{JA}$) (Note 2).....82°C/W
Package Junction-to-Case
Thermal Resistance ($\theta_{JC}$) (Note 2) .....32°C/W
Operating Temperature Range
MAX195_ ESA.....-40°C to +85°C
Junction Temperature Range .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**Note 1:** LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = $V_{CC}$ = 3.3V, PGND = GND, FB in regulation, $C_{REF}$ = 0.1µF, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **IN AND $V_{CC}$** | | | | | | | |
| IN Voltage Range | | | | 2.6 | | 5.5 | V |
| Supply Current | Switching with no load, LX unconnected | | $V_{IN}$ = 5.5V | | 6 | 10 | mA |
| Shutdown Current | COMP = GND | | | | 0.5 | 1.0 | mA |
| $V_{CC}$ Undervoltage Lockout Threshold | When LX starts/stops switching | | $V_{CC}$ rising | | 2.35 | 2.5 | V |
| | | | $V_{CC}$ falling | 2 | 2.25 | | |
| **REF** | | | | | | | |
| REF Voltage | $I_{REF}$ = 0µA, $V_{IN}$ = 2.6V to 5.5V | | | 1.96 | 2 | 2.03 | V |
| REF Load Regulation | $I_{REF}$ = 0 to 40µA, $V_{IN}$ = 2.6V to 5.5V | | | | 0.01 | 0.2 | % |
| REF Line Regulation | $I_{REF}$ = 20µA, $V_{IN}$ = 2.6V to 5.5V | | | | 0.01 | 0.4 | % |
| REF Shutdown Resistance | From REF to GND, COMP = GND | | | | 12 | 22 | Ω |
| **COMP** | | | | | | | |
| COMP Transconductance | From FB to COMP, $V_{COMP}$ = 1.25V | | MAX1951 | 40 | 60 | 80 | µS |
| | | | MAX1952 | 26.7 | 40 | 53.3 | |
| COMP Clamp Voltage, Low | $V_{IN}$ = 2.6V to 5.5V, $V_{FB}$ = 1.3V | | | 0.6 | 1 | 1.2 | V |
| COMP Clamp Voltage, High | $V_{IN}$ = 2.6V to 5.5V, $V_{FB}$ = 1.1V | | | 1.97 | 2.15 | 2.28 | V |
| COMP Shutdown Resistance | From COMP to GND, $V_{IN}$ = 2V | | | | 15 | 30 | Ω |
| COMP Shutdown Threshold | When LX starts/stops switching | | COMP rising | | 0.6 | 1 | V |
| | | | COMP falling | 0.17 | 0.4 | | |
| COMP Startup Current | COMP = GND | | | 15 | 25 | 40 | µA |
| **FB** | | | | | | | |
| Output Voltage Range (MAX1951) | When using external feedback resistors to drive FB | | | 0.8 | | $V_{IN}$ | V |
| FB Regulation Voltage (Error Amp Only) | $V_{COMP}$ = 1V to 2V, $I_{OUT}$ = 0 to 1.5A | $V_{IN}$ = 2.6V to 5.5V | MAX1951 | 0.787 | 0.795 | 0.803 | V |
| | | $V_{IN}$ = 2.8V to 5.5V | MAX1952 | 1.773 | 1.8 | 1.827 | |
| FB Input Resistance | | | MAX1952 | 13 | 18 | 28 | kΩ |
| FB Input Bias Current | | | MAX1951 | -0.1 | | +0.1 | µA |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = $V_{CC}$ = 3.3V, PGND = GND, FB in regulation, $C_{REF}$ = 0.1µF, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **LX** | | | | | | |
| LX On-Resistance, PMOS | $V_{IN}$ = 5V | | | 116 | | mΩ |
| | $V_{IN}$ = 3.3V | | | 140 | 266 | |
| | $V_{IN}$ = 2.6V | | | 163 | | |
| LX On-Resistance, NMOS | $V_{IN}$ = 5V | | | 93 | | mΩ |
| | $V_{IN}$ = 3.3V | | | 106 | 206 | |
| | $V_{IN}$ = 2.6V | | | 116 | | |
| LX Current-Sense Transimpedance | From LX to COMP, $V_{IN}$ = 2.6V to 5.5V | | 0.16 | 0.24 | 0.35 | Ω |
| LX Current-Limit Threshold | Duty cycle = 100%, $V_{IN}$ = 2.6V to 5.5V | High side | 2.4 | 3.1 | 4.5 | A |
| | | Low side | | -0.6 | | |
| LX Leakage Current | $V_{IN}$ = 5.5V | $V_{LX}$ = 5.5V | | | 10 | µA |
| | | LX = GND | -10 | | | |
| LX Switching Frequency | $V_{IN}$ = 2.6V to 5.5V | | 0.85 | 1 | 1.1 | MHz |
| LX Maximum Duty Cycle | $V_{COMP}$ = 1.5V, LX = Hi-Z, $V_{IN}$ = 2.6V to 5.5V | | 100 | | | % |
| LX Minimum Duty Cycle | $V_{COMP}$ = 1V, $V_{IN}$ = 2.6V to 5.5V | | | 15 | | % |
| **THERMAL CHARACTERISTICS** | | | | | | |
| Thermal-Shutdown Threshold | When LX starts/stops switching | $T_J$ rising | | 160 | | °C |
| | | $T_J$ falling | | 145 | | |

## ELECTRICAL CHARACTERISTICS

($V_{IN}$ = $V_{CC}$ = 3.3V, PGND = GND, FB in regulation, $C_{REF}$ = 0.1µF, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 3)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **IN AND $V_{CC}$** | | | | | | |
| IN Voltage Range | | | 2.6 | | 5.5 | V |
| Supply Current | Switching with no load, $V_{IN}$ = 5.5V | | | | 10 | mA |
| Shutdown Current | COMP = GND | | | | 1 | mA |
| $V_{CC}$ Undervoltage Lockout Threshold | When LX starts/stops switching | $V_{CC}$ rising | | | 2.5 | V |
| | | $V_{CC}$ falling | 1.95 | | | |
| **REF** | | | | | | |
| REF Voltage | $I_{REF}$ = 0µA, $V_{IN}$ = 2.6V to 5.5V | | 1.95 | | 2.03 | V |
| REF Load Regulation | $I_{REF}$ = 0 to 40µA, $V_{IN}$ = 2.6V to 5.5V | | | | 0.2 | % |
| REF Line Regulation | $I_{REF}$ = 20µA, $V_{IN}$ = 2.6V to 5.5V | | | | 0.4 | % |
| REF Shutdown Resistance | From REF to GND, COMP = GND | | | | 22 | Ω |

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

## ELECTRICAL CHARACTERISTICS (continued)

($V_{IN}$ = $V_{CC}$ = 3.3V, PGND = GND, FB in regulation, $C_{REF}$ = 0.1µF, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 3)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **COMP** | | | | | | |
| COMP Transconductance | From FB to COMP, $V_{COMP}$ = 1.25V | MAX1951 | 40 | | 80 | µS |
| | | MAX1952 | 26.7 | | 53.3 | |
| COMP Clamp Voltage, Low | $V_{IN}$ = 2.6V to 5.5V, $V_{FB}$ = 1.3V | | 0.6 | | 1.2 | V |
| COMP Clamp Voltage, High | $V_{IN}$ = 2.6V to 5.5V, $V_{FB}$ = 1.1V | | 1.97 | | 2.28 | V |
| COMP Shutdown Resistance | From COMP to GND, $V_{IN}$ = 2V | | | | 30 | Ω |
| COMP Shutdown Threshold | When LX starts/stops switching | COMP rising | | | 1.2 | V |
| | | COMP falling | 0.17 | | | |
| COMP Startup Current | COMP = GND | | 14 | | 40 | µA |
| **FB** | | | | | | |
| Output Voltage Range (MAX1951) | When using external feedback resistors to drive FB | | 0.8 | | $V_{IN}$ | V |
| FB Regulation Voltage (Error Amp Only) | $V_{COMP}$ = 1V to 2V, $V_{IN}$ = 2.6V to 5.5V | MAX1951 | 0.783 | | 0.807 | V |
| | | MAX1952 | 1.764 | | 1.836 | |
| FB Input Resistance | From FB to GND | MAX1952 | 10 | | 30 | kΩ |
| FB Input Bias Current | | MAX1951 | -0.1 | | +0.1 | µA |
| **LX (Note 4)** | | | | | | |
| LX On-Resistance, PMOS | | | | | 266 | mΩ |
| LX On-Resistance, NMOS | | | | | 206 | mΩ |
| LX Current Sense | From LX to COMP, $V_{IN}$ = 2.6V to 5.5V | | 0.16 | | 0.35 | Ω |
| LX Current-Limit Threshold | Duty cycle = 100%, $V_{IN}$ = 2.6V to 5.5V, high side | | 2.4 | | 4.5 | A |
| LX Leakage Current | $V_{IN}$ = 5.5V | $V_{LX}$ = 5.5V | | | 10 | µA |
| | | LX = GND | -10 | | | |
| LX Switching Frequency | $V_{IN}$ = 2.6V to 5.5V | | 0.8 | | 1.1 | MHz |
| LX Maximum Duty Cycle | $V_{COMP}$ = 1.5V, LX = Hi-Z, $V_{IN}$ = 2.6V to 5.5V | | 100 | | | % |

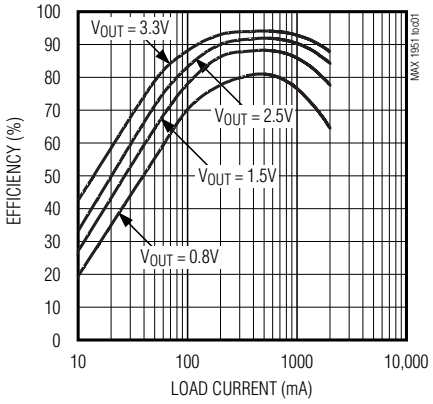
**Note 3:** Specifications to -40°C are guaranteed by design and not production tested.
**Note 4:** The LX output is designed to provide 2.4A RMS current.

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

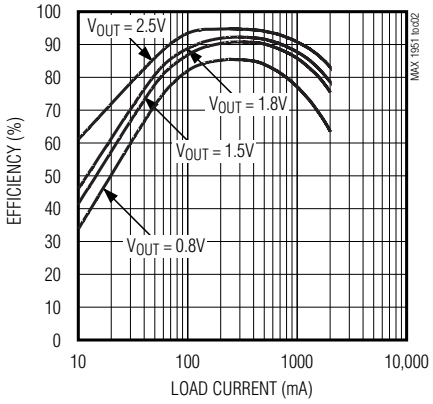
## Typical Operating Characteristics

(Typical values are at $V_{IN}$ = $V_{CC}$ = 5V, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 1.5A, and $T_A$ = +25°C, unless otherwise noted. See Figure 2.)

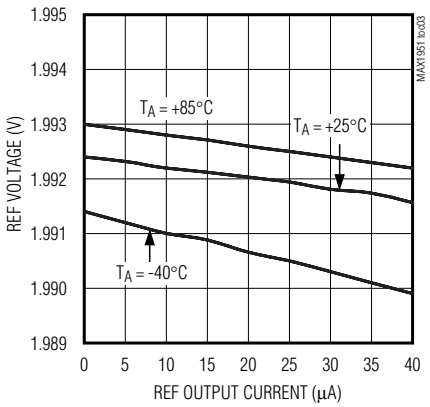
**EFFICIENCY vs. LOAD CURRENT ($V_{CC}$ = $V_{IN}$ = 5V)**



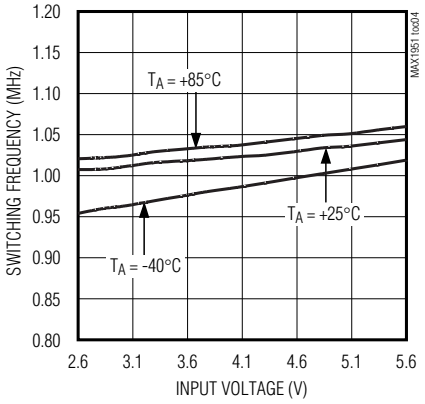

**EFFICIENCY vs. LOAD CURRENT ($V_{CC}$ = $V_{IN}$ = 3.3V)**



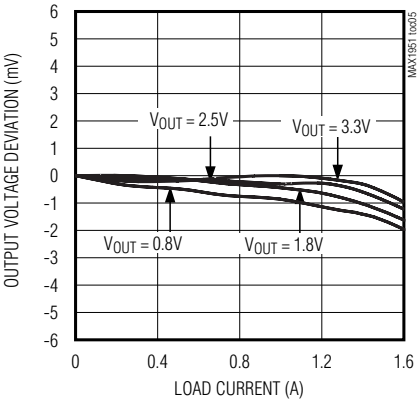

**REF VOLTAGE vs. REF OUTPUT CURRENT**



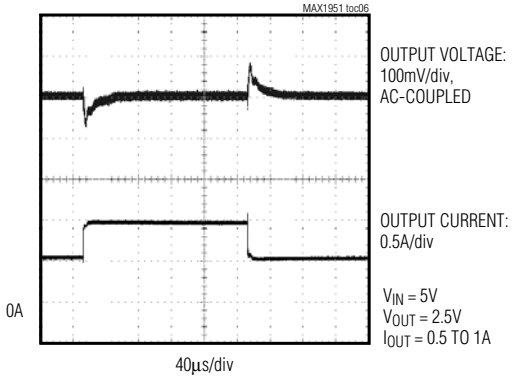

**SWITCHING FREQUENCY vs. INPUT VOLTAGE**



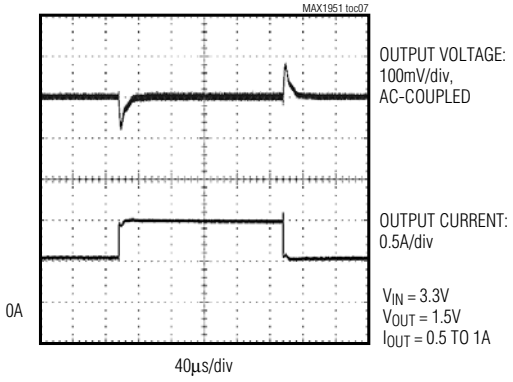

**OUTPUT VOLTAGE DEVIATION vs. LOAD CURRENT**




**LOAD-TRANSIENT RESPONSE**




**LOAD-TRANSIENT RESPONSE**

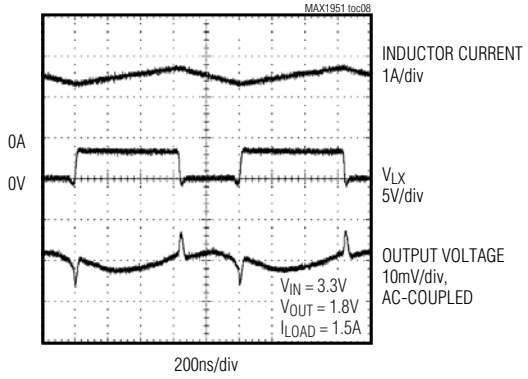


# 1MHz, All Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

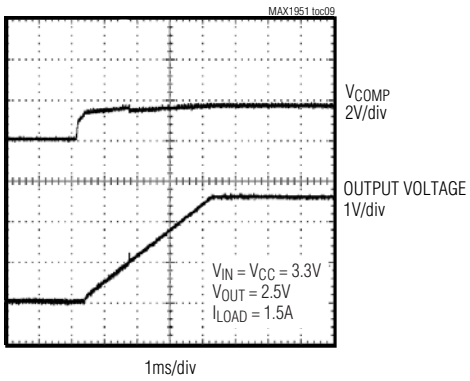
## Typical Operating Characteristics (continued)

(Typical values are at $V_{IN}$ = $V_{CC}$ = 5V, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 1.5A, and $T_A$ = +25°C, unless otherwise noted. See Figure 2.)

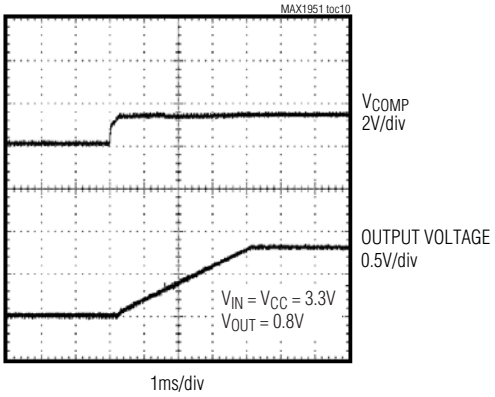
**SWITCHING WAVEFORMS**



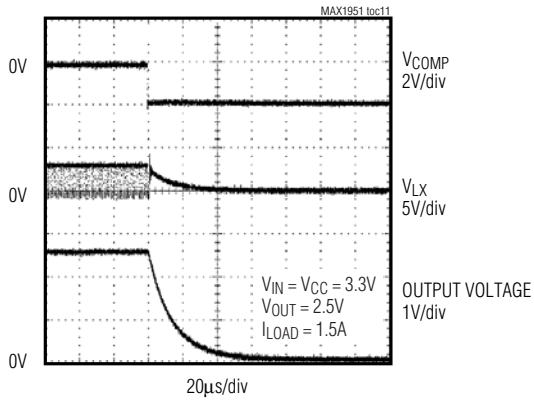

**SOFT-START WAVEFORMS**



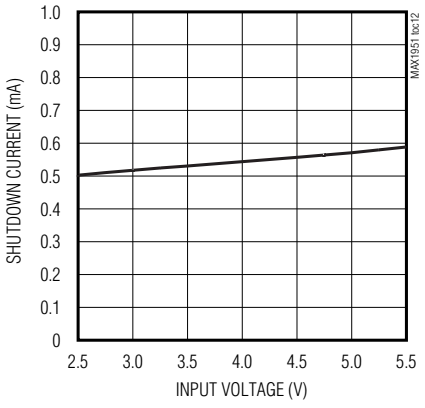

**SOFT-START WAVEFORMS**




**SHUTDOWN WAVEFORMS**




**SHUTDOWN CURRENT vs. INPUT VOLTAGE**



## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{CC}$ | Supply Voltage. Bypass $V_{CC}$ with 0.1µF capacitor to ground and 10Ω resistor to IN. |
| 2 | REF | Reference Bypass. Bypass REF with 0.1µF capacitor to ground. |
| 3 | GND | Ground |
| 4 | FB | Feedback Input. Connect FB to the output to regulate using the internal feedback resistor string (MAX1952). Connect an external resistor-divider from the output to FB and GND to set the output to a voltage between 0.8V and $V_{IN}$ (MAX1951). |
| 5 | COMP | Regulator Compensation. Connect series RC network from COMP to GND. Pull COMP below 0.17V to shut down the regulator. COMP = GND when $V_{IN}$ is less than 2.25V (see the *Compensation and Shutdown Mode* section) |
| 6 | PGND | Power Ground. Internally connected to GND. Keep power ground and signal ground planes separate. |
| 7 | LX | Inductor Connection. Connect an inductor between LX and the regulator output. |
| 8 | IN | Power-Supply Voltage. Input voltage range from 2.6V to 5.5V. Bypass IN with a 10µF (min) ceramic capacitor to GND and a 10Ω resistor to $V_{CC}$. |

## Detailed Description

The MAX1951/MAX1952 high-efficiency switching regulators are small, simple, DC-to-DC step-down converters capable of delivering up to 2A of output current. The devices operate in pulse-width modulation (PWM) at a fixed frequency of 1MHz from a 2.6V to 5.5V input voltage and provide an output voltage from 0.8V to $V_{IN}$, making the MAX1951/MAX1952 ideal for on-board postregulation applications. The high switching frequency allows for the use of smaller external components, and internal synchronous rectifiers improve efficiency and eliminate the typical Schottky free-wheeling diode. Using the on-resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost. The MAX1951 total output error over load, line, and temperature (0°C to +85°C) is less than 1%.

### Controller Block Function

The MAX1951/MAX1952 step-down converters use a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator trips. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (<30% ripple current), the circuit acts as a switch-mode transconductance amplifier. To preserve inner-loop stability and eliminate inductor staircasing, a slope-compensation ramp is summed into the main PWM comparator. During the second half of the cycle, the internal high-side p-channel MOSFET turns off, and the internal low-side n-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current, and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the current limit (see the *Current Limit* section), the high-side MOSFET does not turn on at the rising edge of the clock and the low-side MOSFET remains on to let the inductor current ramp down.

### Current Sense

An internal current-sense amplifier produces a current signal proportional to the voltage generated by the high-side MOSFET on-resistance and the inductor current ($R_{DS(ON)} \times I_{LX}$). The amplified current-sense signal and the internal slope compensation signal are summed together into the comparator's inverting input. The PWM comparator turns off the internal high-side MOSFET when this sum exceeds the output from the voltage-error amplifier.

### Current Limit

The internal high-side MOSFET has a current limit of 3.1A (typ). If the current flowing out of LX exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. This lowers the duty cycle and causes the output voltage to droop until the current limit is no longer exceeded. A synchronous rectifier current limit of -0.6A (typ) protects the device from current flowing into LX. If the negative current limit is exceeded, the synchronous rectifier turns off, forcing the inductor current to flow

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

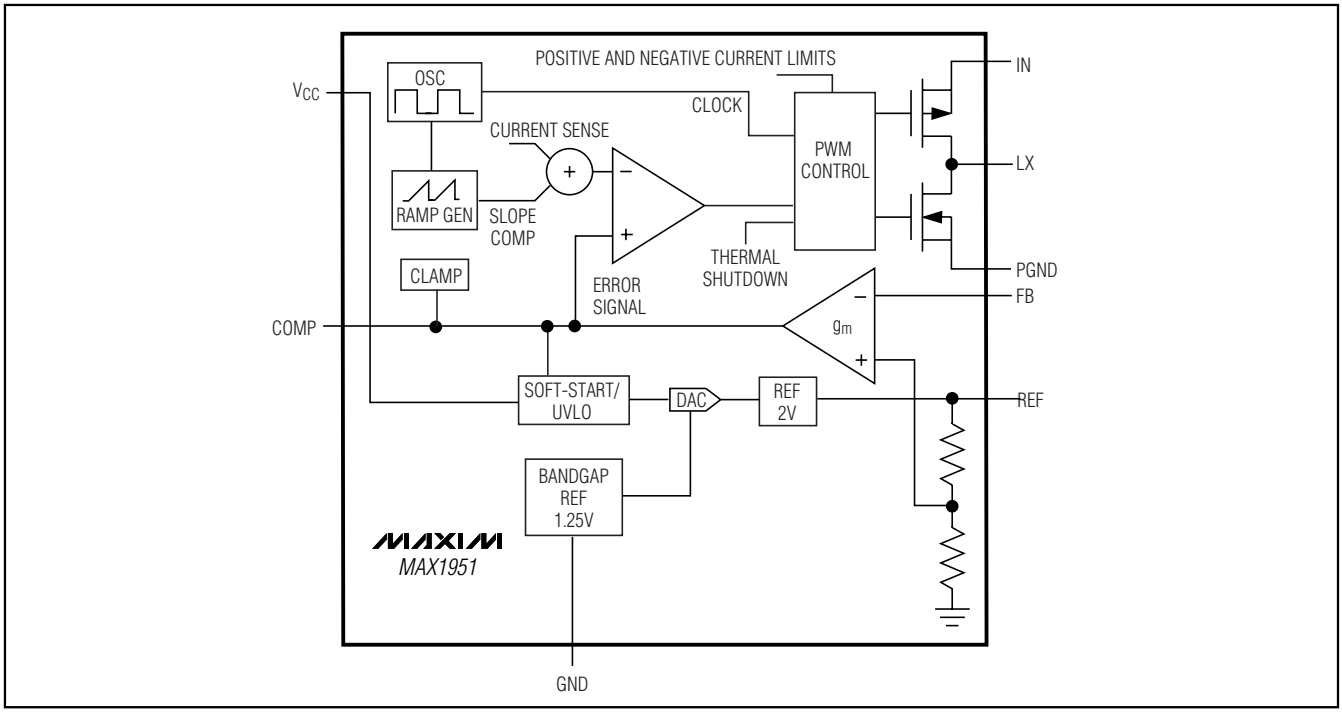



*Figure 1. Functional Diagram*

through the high-side MOSFET body diode, back to the input, until the beginning of the next cycle or until the inductor current drops to zero. The MAX1951/MAX1952 utilize a pulse-skip mode to prevent overheating during short-circuit output conditions. The device enters pulse-skip mode when the FB voltage drops below 300mV, limiting the current to 3A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

### $V_{CC}$ Decoupling

Due to the high switching frequency and tight output tolerance (1%), decouple $V_{CC}$ with a 0.1µF capacitor connected from $V_{CC}$ to GND, and a 10Ω resistor connected from $V_{CC}$ to IN. Place the capacitor as close to $V_{CC}$ as possible.

### Soft-Start

The MAX1951/MAX1952 employ digital soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits undervoltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, or the external pulldown on COMP is released, the digital soft-start circuitry slowly ramps up the voltages at REF and FB (see the Soft-Start Waveforms in the *Typical Operating Characteristics)*.

### Undervoltage Lockout

If $V_{CC}$ drops below 2.25V, the UVLO circuit inhibits switching. Once $V_{CC}$ rises above 2.35V, the UVLO clears, and the soft-start sequence activates.

### Compensation and Shutdown Mode

The output of the internal transconductance voltage error amplifier connects to COMP. The normal operation voltage for COMP is 1V to 2.2V. To shut down the MAX1951/MAX1952, use an NPN bipolar junction transistor or a very low output capacitance open-drain MOSFET to pull COMP to GND. Shutdown mode causes the internal MOSFETs to stop switching, forces LX to a high-impedance state, and shorts REF to GND. Release COMP to exit shutdown and initiate the soft-start sequence.

### Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds $T_J$ = +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

## Design Procedure

### Output Voltage Selection: Adjustable (MAX1951) or Preset (MAX1952)

The MAX1951 provides an adjustable output voltage between 0.8V and $V_{IN}$. Connect FB to output for 0.8V output. To set the output voltage of the MAX1951 to a voltage greater than $V_{FB}$ (0.8V typ), connect the output to FB and GND using a resistive divider, as shown in Figure 2a. Choose R2 between 2kΩ and 20kΩ, and set R3 according to the following equation:

$$R3 = R2 \times [(V_{OUT}/V_{FB}) - 1]$$

The MAX1951 PWM circuitry is capable of a stable minimum duty cycle of 18%. This limits the minimum output voltage that can be generated to $0.18 \times V_{IN}$. Instability may result for $V_{IN}/V_{OUT}$ ratios below 0.18.

The MAX1952 provides a preset output voltage. Connect the output to FB, as shown in Figure 2b.

### Output Inductor Design

Use a 2µH inductor with a minimum 2A-rated DC current for most applications. For best efficiency, use an inductor with a DC resistance of less than 20mΩ and a saturation current greater than 3A (min). See Table 2 for recommended inductors and manufacturers. For most designs, derive a reasonable inductor value ($L_{INIT}$) from the following equation:

$$L_{INIT} = V_{OUT} \times (V_{IN} - V_{OUT})/(V_{IN} \times LIR \times I_{OUT(MAX)} \times f_{SW})$$

where $f_{SW}$ is the switching frequency (1MHz typ) of the oscillator. Keep the inductor current ripple percentage LIR between 20% and 40% of the maximum load current for the best compromise of cost, size, and performance. Calculate the maximum inductor current as:

$$I_{L(MAX)} = (1 + LIR/2) \times I_{OUT(MAX)}$$

Check the final values of the inductor with the output ripple voltage requirement. The output ripple voltage is given by:

$$V_{RIPPLE} = V_{OUT} \times (V_{IN} - V_{OUT}) \times ESR / (V_{IN} \times L_{FINAL} \times f_{SW})$$

where ESR is the equivalent series resistance of the output capacitors.

### Input Capacitor Design

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor must meet the ripple current requirement ($I_{RMS}$) imposed by the switching currents defined by the following equation:

$$I_{RMS} = (1/V_{IN}) \times \sqrt{(I_{OUT}^2 \times V_{OUT} \times (V_{IN} - V_{OUT}))}$$

For duty ratios less than 0.5, the input capacitor RMS current is higher than the calculated current. Therefore, use a +20% margin when calculating the RMS current at lower duty cycles. Use ceramic capacitors for their low ESR, equivalent series inductance (ESL), and lower cost. Choose a capacitor that exhibits less than 10°C temperature rise at the maximum operating RMS current for optimum long-term reliability.

After determining the input capacitor, check the input ripple voltage due to capacitor discharge when the high-side MOSFET turns on. Calculate the input ripple voltage as follows:

$$V_{IN_RIPPLE} = (I_{OUT} \times V_{OUT})/(f_{SW} \times V_{IN} \times C_{IN})$$

Keep the input ripple voltage less than 3% of the input voltage.

### Output Capacitor Design

The key selection parameters for the output capacitor are capacitance, ESR, ESL, and the voltage rating requirements. These affect the overall stability, output ripple voltage, and transient response of the DC-to-DC converter. The output ripple occurs due to variations in the charge stored in the output capacitor, the voltage drop due to the capacitor's ESR, and the voltage drop due to the capacitor's ESL. Calculate the output voltage ripple due to the output capacitance, ESR, and ESL as:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)} + V_{RIPPLE(ESL)}$$

where the output ripple due to output capacitance, ESR, and ESL is:

$$V_{RIPPLE(C)} = I_{P-P}/(8 \times C_{OUT} \times f_{SW})$$

$$V_{RIPPLE(ESR)} = I_{P-P} \times ESR$$

$$V_{RIPPLE(ESL)} = (I_{P-P}/t_{ON}) \times ESL \text{ or } (I_{P-P}/t_{OFF}) \times ESL, \text{ whichever is greater}$$

and $I_{P-P}$ the peak-to-peak inductor current is:

$$I_{P-P} = [\ (V_{IN} - V_{OUT})/f_{SW} \times L)\ ] \times V_{OUT}/V_{IN}$$

Use these equations for initial capacitor selection, but determine final values by testing a prototype or evaluation circuit. As a rule, a smaller ripple current results in less output voltage ripple. Since the inductor ripple current is a factor of the inductor value, the output voltage ripple decreases with larger inductance. Use ceramic capacitors for their low ESR and ESL at the switching frequency of the converter. The low ESL of ceramic capacitors makes ripple voltages negligible. Load transient response depends on the selected output capacitor. During a load transient, the output instantly changes by ESR x $I_{LOAD}$. Before the controller can respond, the output deviates further, depending on the inductor and output capacitor values. After a short time (see the Load Transient Response graph in the

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

*Typical Operating Characteristic*s), the controller responds by regulating the output voltage back to its nominal state. The controller response time depends on the closed-loop bandwidth. A higher bandwidth yields a faster response time, thus preventing the output from deviating further from its regulating value.

### Compensation Design

The double pole formed by the inductor and output capacitor of most voltage-mode controllers introduces a large phase shift, that requires an elaborate compensation network to stabilize the control loop. The MAX1951/MAX1952 utilize a current-mode control scheme that regulates the output voltage by forcing the required current through the external inductor, eliminating the double pole caused by the inductor and output capacitor, and greatly simplifying the compensation network. A simple type 1 compensation with single compensation resistor ($R_1$) and compensation capacitor ($C_2$) creates a stable and high-bandwidth loop.

An internal transconductance error amplifier compensates the control loop. Connect a series resistor and capacitor between COMP (the output of the error amplifier) and GND to form a pole-zero pair. The external inductor, internal current-sensing circuitry, output capacitor, and the external compensation circuit determine the loop system stability. Choose the inductor and output capacitor based on performance, size, and cost. Additionally, select the compensation resistor and capacitor to optimize control-loop stability. The component values shown in the typical application circuit (Figure 2) yield stable operation over a broad range of input-to-output voltages.

The basic regulator loop consists of a power modulator, an output feedback divider, and an error amplifier. The power modulator has DC gain set by gmc x $R_{LOAD}$, with a pole-zero pair set by $R_{LOAD}$, the output capacitor ($C_{OUT}$), and its ESR. The following equations define the power modulator:

Modulator gain:

$$G_{MOD} = \Delta V_{OUT}/\Delta V_{COMP} = gmc \times R_{LOAD}$$

Modulator pole frequency:

$$fp_{MOD} = 1 / (2 \times \pi \times C_{OUT} \times (R_{LOAD}+ESR))$$

Modulator zero frequency:

$$fz_{ESR} = 1 /(2 \times \pi \times C_{OUT} \times ESR)$$

where, $R_{LOAD} = V_{OUT}/I_{OUT(MAX)}$, and gmc = 4.2S.

The feedback divider has a gain of $G_{FB} = V_{FB} / V_{OUT}$, where $V_{FB}$ is equal to 0.8V. The transconductance error amplifier has a DC gain, $G_{EA(DC)}$, of 70dB. The compensation capacitor, $C_2$, and the output resistance of the error amplifier, $R_{OEA}$ (20MΩ), set the dominant pole. $C_2$ and $R_1$ set a compensation zero. Calculate the dominant pole frequency as:

$$fp_{EA} = 1/(2\pi x C_C x R_{OEA})$$

Determine the compensation zero frequency is:

$$fz_{EA} = 1/(2\pi \times C_C \times R_C)$$

For best stability and response performance, set the closed-loop unity-gain frequency much higher than the modulator pole frequency. In addition, set the closed-loop crossover unity-gain frequency less than, or equal to, 1/5 of the switching frequency. However, set the maximum zero crossing frequency to less than 1/3 of the zero frequency set by the output capacitance and its ESR when using POSCAP, SPCAP, OSCON, or other electrolytic capacitors.The loop-gain equation at the unity-gain frequency is:

$$G_{EA(fc)} \times G_{MOD(fc)} \times V_{FB}/V_{OUT} = 1$$

where $G_{EA(fc)} = gm_{EA} \times R_1$, and $G_{MOD(fc)} = gmc \times R_{LOAD} \times fp_{MOD}/f_C$, where $gm_{EA}$ = 60µS.

$R_1$ calculated as:

$$R_1 = V_{OUT} \times K/(gm_{EA} \times V_{FB} \times G_{MOD(fc)})$$

where K is the correction factor due to the extra phase introduced by the current loop at high frequencies (>100kHz). K is related to the value of the output capacitance (see Table 1 for values of K vs. C). Set the error-amplifier compensation zero formed by $R_1$ and $C_2$ at the modulator pole frequency at maximum load. $C_2$ is calculated as follows:

$$C_2 = (V_{OUT} \times C_{OUT}/(R_1 \times I_{OUT(MAX)}))$$

As the load current decreases, the modulator pole also decreases; however, the modulator gain increases accordingly, resulting in a constant closed-loop unity-gain frequency. Use the following numerical example to calculate $R_1$ and $C_2$ values of the typical application circuit of Figure 2a.

## Table 1. K Value

| | | DESCRIPTION |
|---|---|---|
| $C_{OUT}$ (µF) | K | Values are for output inductance from 1.2µH to 2.2µH. Do not use output inductors larger than 2.2µH. Use $f_C$ = 200kHz to calculate $R_1$. |
| 10 | 0.55 | |
| 22 | 0.47 | |

$V_{OUT}$ = 1.5V

$I_{OUT(MAX)}$ = 1.5A

$C_{OUT}$ = 10µF

$R_{ESR}$ = 0.010Ω

$gm_{EA}$ = 60µS

gmc = 4.2S

$f_{SWITCH}$ = 1MHz

$R_{LOAD} = V_{OUT}/I_{OUT(MAX)} = 1.5V/1.5\ A = 1\Omega$

$fp_{MOD} = [1/(2\pi \times C_{OUT} \times (R_{LOAD} + R_{ESR})]$
$= [1/(2 \times \pi \times 10 \times 10^{-6} \times (1 + 0.01)] = 15.76kHz.$

$fz_{ESR} = [1/(2\pi \times C_{OUT} R_{ESR})]$
$= [1/(2 \times \pi \times 10 \times 10^{-6} \times 0.01)] = 1.59MHz.$

For 2µH output inductor, pick the closed-loop unity-gain crossover frequency ($f_C$) at 200kHz. Determine the power modulator gain at $f_C$:

$$G_{MOD(fc)} = gmc \times R_{LOAD} \times fp_{MOD}/f_C = 4.2 \times 1 \times 15.76kHz/200kHz = 0.33$$

then:

$$R_1 = V_O \times K/(gm_{EA} \times V_{FB} \times G_{MOD(fc)}) = (1.5 \times 0.55)/(60 \times 10^{-6} \times 0.8 \times 0.33) \approx 51.1k\Omega\ (1\%)$$

$$C_2 = (V_{OUT} \times C_{OUT})/(R \times I_{OUT(max)}) = (1.5 \times 10 \times 10^{-6})/(51.1k \times 1.5) \approx 196pF,\ \text{choose}\ 220pF,\ 10\%$$

## Applications Information

### PCB Layout Considerations

Careful PCB layout is critical to achieve clean and stable operation. The switching power stage requires particular attention. Follow these guidelines for good PCB layout:

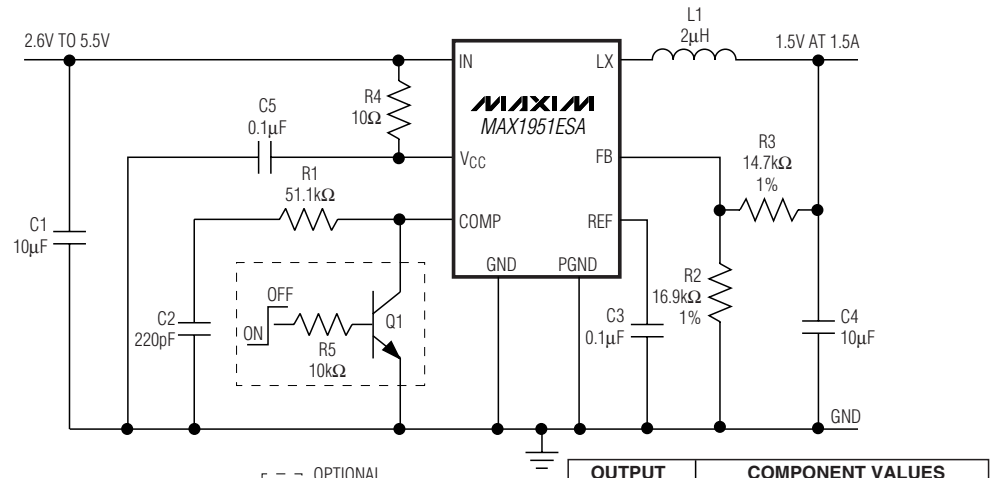
1) Place decoupling capacitors as close to the IC as possible. Keep power ground plane (connected to PGND) and signal ground plane (connected to GND) separate.
2) Connect input and output capacitors to the power ground plane; connect all other capacitors to the signal ground plane.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (C1 to IN and C1 to PGND) short. Avoid vias in the switching paths.
4) If possible, connect IN, LX, and PGND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas (FB, COMP).

### Thermal Considerations

The MAX1951 uses a fused-lead 8-pin SO package with a $R_{THJC}$ rating of 32°C/W. The MAX1951 EV kit layout is optimized for 1.5A. The typical application circuit shown in Figure 2c was tested with the existing MAX1951 EV kit layout at +85°C ambient temperature, and GND lead temperature was measured at +113°C for a typical device. The estimated junction temperature was +138°C. Thermal performance can be further improved with one of the following options:

1) Increase the copper areas connected to GND, LX, and IN.
2) Provide thermal vias next to GND and IN, to the ground plane and power plane on the back side of PCB, with openings in the solder mask next to the vias to provide better thermal conduction.
3) Provide forced-air cooling to further reduce case temperature.

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators




| OUTPUT VOLTAGE (V) | COMPONENT VALUES | | | |
|---|---|---|---|---|
| | R1 (kΩ) | R2 (kΩ) | R3 (kΩ) | C2 (pF) |
| 0.8 | 33.2 | OPEN | SHORT | 220 |
| 1.5 | 51.1 | 16.9 | 14.7 | 220 |
| 2.5 | 82.5 | 14 | 30 | 220 |
| 3.3 | 110 | 24 | 75 | 220 |

*Figure 2a. MAX1951 Adjustable Output Typical Application Circuit*

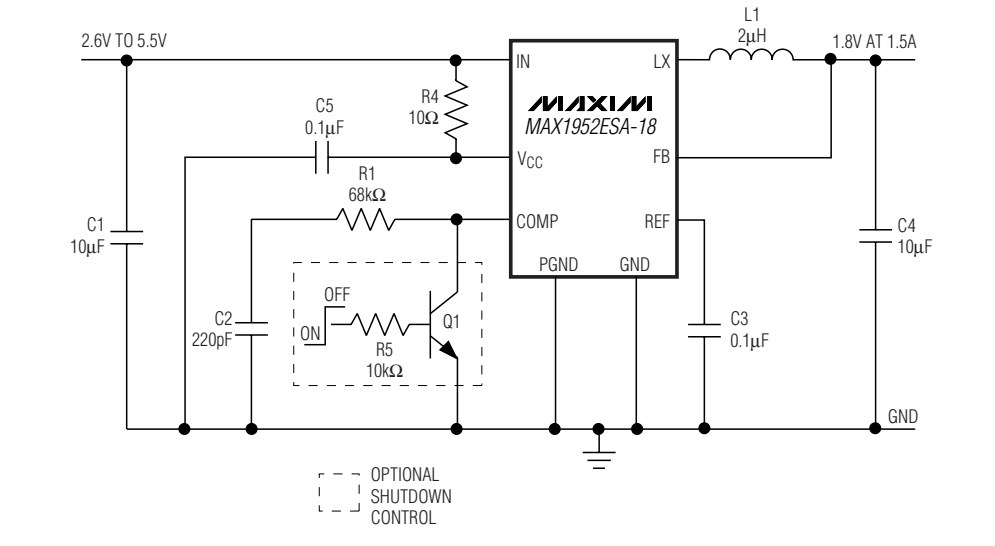



*Figure 2b. MAX1952 Fixed-Output Typical Application Circuit*

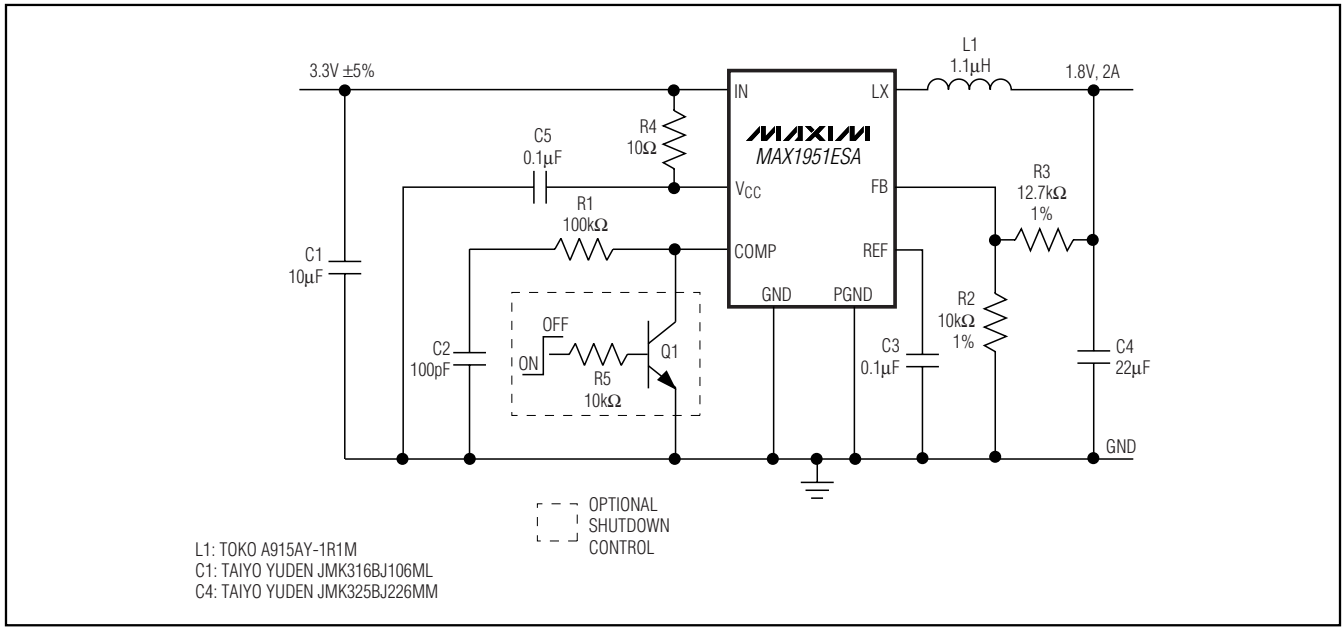



*Figure 2c. MAX1951 Typical Application Circuit with 2A Output*

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

## Table 2. External Components List

| COMPONENT (FIGURE 2) | FUNCTION | DESCRIPTION |
|---|---|---|
| L1 | Output inductor | 2µH ±20% inductor<br>Sumida CDRH4D28-1R8 or<br>Toko A915AY-2R0M |
| C1 | Input filtering capacitor | 10µF ±20%, 6.3V X5R capacitor<br>Taiyo Yuden JMK316BJ106ML or<br>TDK C3216X5R0J106MT |
| C2 | Compensation capacitor | 220pF ±10%, 50V capacitor<br>Murata GRM39X7R221K050AD or<br>Taiyo Yuden UMK107CH221KZ |
| C3 | Reference bypass capacitor | 0.1µF ±20%, 16V X7R capacitor<br>Taiyo Yuden EMK107BJ104MA,<br>TDK C1608X7R1C104K, or<br>Murata GRM 39X7R104K016AD |
| C4 | Output filtering capacitor | 10µF ±20%, 6.3V X5R capacitor<br>Taiyo Yuden JMK316BJ106ML or<br>TDK C3216X5R0J106MT |
| C5 | $V_{CC}$ bypass capacitor | 0.1µF ±20%, 16V X7R capacitor<br>Taiyo Yuden EMK107BJ104MA,<br>TDK C1608X7R1C104K, or<br>Murata GRM 39X7R104K016AD |
| R1 | Loop compensation resistor | Figure 2a |
| R2 | Feedback resistor | Figure 2a |
| R3 | Feedback resistor | Figure 2a |
| R4 | Bypass resistor | 10Ω ±5% resistor |
| R5 | Shutdown transistor base current bias (optional) | 10kΩ ±5% resistor |
| Q1 | Shutdown transistor (optional) | NPN bipolar junction transistor<br>Fairchild MMBT3904<br>Zetex FMMT413 |

## Table 3. Component Suppliers

| MANUFACTURER | PHONE | FAX |
|---|---|---|
| Murata | 650-964-6321 | 650-964-8165 |
| Sumida | 847-545-6700 | 847-545-6720 |
| Taiyo Yuden | 800-348-2496 | 847-925-0899 |
| TDK | 847-803-6100 | 847-803-6296 |
| Toko | 1-800-PIK-TOKO | 408-943-9790 |

## Chip Information

PROCESS: BiCMOS

## Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO. |
|---|---|---|
| 8 SO | S8-F6 | 21-0041 |

# 1MHz, All-Ceramic, 2.6V to 5.5V Input, 2A PWM Step-Down DC-to-DC Regulators

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/02 | Initial release | — |
| 1 | 8/03 | Updated data sheet title, *Features*, *Typical Operating Circuit*, *Detailed Description* and added *Thermal Considerations* section. | 1–15 |
| 2 | 6/09 | Revised *Ordering Information*, *Electrical Characteristics*, *Typical Operating Characteristics*, *Pin Description*, and the *Compensation Design* section. | 1–7, 10, 11, 14 |

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