



LM7001J, 7001JM

Direct PLL Frequency Synthesizers for Electronic Tuning

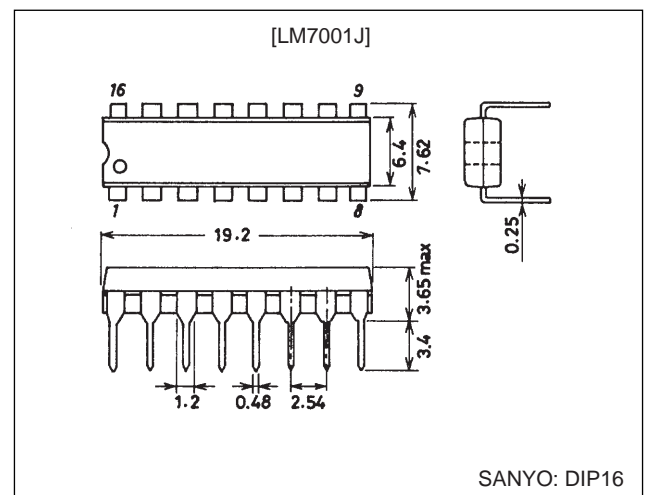
Features

- The LM7001J and LM7001JM are PLL frequency synthesizer LSIs for tuners, making it possible to make up high-performance AM/FM tuners easily.
- These LSIs are software compatible with the LM7000, but do not include an IF calculation circuit.
- The FM VCO circuit includes a high-speed programmable divider that can divide directly.
- Seven reference frequencies: 1, 5, 9, 10, 25, 50, and 100 kHz
- Band-switching outputs (3 bits)
- Controller clock output (400 kHz)
- Clock time base output (8 Hz)
- Serial input circuit for data input (using the CE, CL, and DATA pins)

Package Dimensions

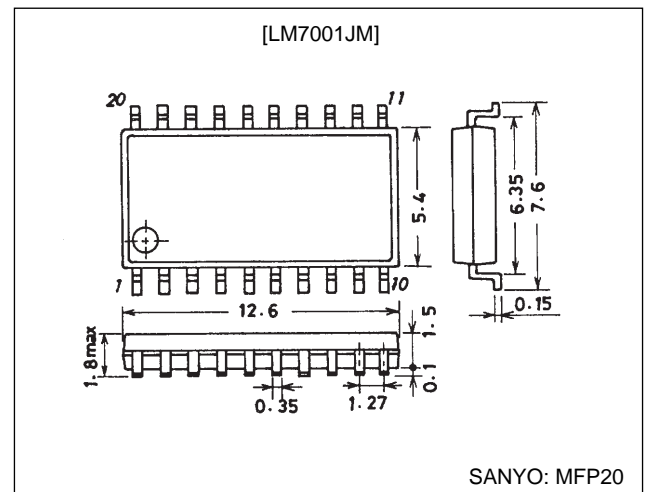
unit: mm

3006B-DIP16



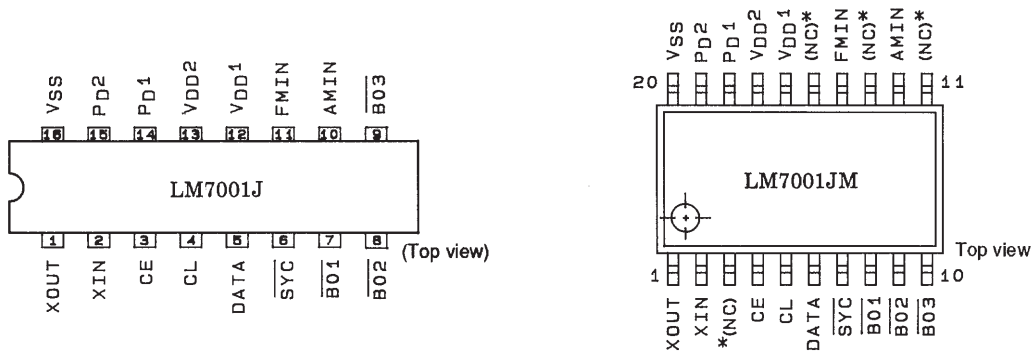
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3036B-MFP20



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Pin Assignments



Note: * NC pins must be left open.

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|-----------------------|--|------------------------|------------------|
| Maximum supply voltage | $V_{DD\text{ max}}$ | V_{DD1} , V_{DD2} | -0.3 to +7.0 | V |
| Maximum input voltage | $V_{IN1\text{ max}}$ | CE, CL, DATA | -0.3 to +7.0 | V |
| | $V_{IN2\text{ max}}$ | Input pins other than V_{IN1} | -0.3 to $V_{DD} + 0.3$ | V |
| Maximum output voltage | $V_{OUT1\text{ max}}$ | $\overline{\text{SYNC}}$ | -0.3 to +7.0 | V |
| | $V_{OUT2\text{ max}}$ | $\overline{\text{B01}}$ to $\overline{\text{B03}}$ | -0.3 to +13 | V |
| | $V_{OUT3\text{ max}}$ | Output pins other than V_{OUT1} and V_{OUT2} | -0.3 to $V_{DD} + 0.3$ | V |
| Maximum output current | $I_{OUT\text{ max}}$ | $\overline{\text{B01}}$ to $\overline{\text{B03}}$ | 0 to 3.0 | mA |
| Allowable power dissipation | $P_d\text{ max}$ | $T_a = 85^\circ\text{C}$: LM7001J (DIP16) | 300 | mW |
| | | $T_a = 85^\circ\text{C}$: LM7001JM (MFP20) | 180 | mW |
| Operating temperature | T_{opr} | | -40 to +85 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +125 | $^\circ\text{C}$ |

Allowable Operating Ranges at $T_a = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|--|------------|---|-----------------------|------|
| Supply voltage | V_{DD1} | V_{DD1} , PLL circuit operating | 4.5 to 6.5 | V |
| | V_{DD2} | V_{DD2} , crystal oscillator time base | 3.5 to 6.5 | V |
| Input high-level voltage | V_{IH} | CE, CL, DATA | 2.2 to 6.5 | V |
| Input low-level voltage | V_{IL} | CE, CL, DATA | 0 to 0.7 | V |
| Output voltage | V_{OUT1} | $\overline{\text{SYNC}}$ | 0 to 6.5 | V |
| | V_{OUT2} | $\overline{\text{B01}}$ to $\overline{\text{B03}}$ | 0 to 13 | V |
| Output current | I_{OUT} | $\overline{\text{B01}}$ to $\overline{\text{B03}}$, $V_{DD} = 4.5$ to 6.5 V | 0 to 3.0 | mA |
| Input frequency | f_{IN1} | XIN, sine wave, capacitor coupled | 1.0 to 7.2 typ to 8.0 | MHz |
| | f_{IN2} | FMIN, sine wave, capacitor coupled*1, $s^{*3} = 1$ | 45 to 130 | MHz |
| | f_{IN3} | FMIN, sine wave, capacitor coupled*2, $s^{*3} = 1$ | 5 to 30 | MHz |
| | f_{IN4} | AMIN, sine wave, capacitor coupled, $s^{*3} = 0$ | 0.5 to 10 | MHz |
| Crystal element for guaranteed oscillation | Xtal | XIN to XOUT, $C_I \leq 30\ \Omega$ | 5.0 to 7.2 typ to 8.0 | MHz |
| Input amplitude | V_{IN1} | XIN, sine wave, capacitor coupled | 0.5 to 1.5 | Vrms |
| | V_{IN2} | FMIN, sine wave, capacitor coupled | 0.1 to 1.5 | Vrms |
| | V_{IN3} | AMIN, sine wave, capacitor coupled | 0.1 to 1.5 | Vrms |

Note: 1. $f_{ref} = 25, 50, \text{ or } 100\text{ kHz}$
 2. $f_{ref} = \text{Reference frequencies other than those for } *1.$
 3. "s" refers to the control bit in the serial data.

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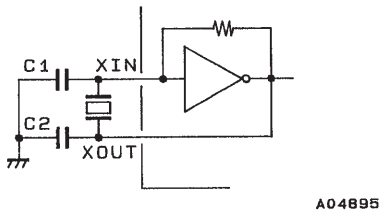
Electrical Characteristics in the Allowable Operating Ranges

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--|------------|--|--------------|------|------|---------------|
| Built-in feedback resistance | R_{f1} | XIN | | 1.0 | | $M\Omega$ |
| | R_{f2} | FMIN | | 500 | | $k\Omega$ |
| | R_{f3} | AMIN | | 500 | | $k\Omega$ |
| Input high-level current | I_{IH} | CE, CL, DATA: $V_{IN} = 6.5\text{ V}$ | | | 5.0 | μA |
| Input low-level current | I_{IL} | CE, CL, DATA: $V_{IN} = 0\text{ V}$ | | | 5.0 | μA |
| Output low-level voltage | V_{OL1} | FMIN, AMIN: $I_{OUT} = 0.5\text{ mA}$ | | | 3.5 | V |
| | V_{OL2} | $\overline{\text{SYC}}$: $I_{OUT} = 0.1\text{ mA}$, *1 | 0.02 | | 0.3 | V |
| | V_{OL3} | $\overline{\text{BO1}}$ to $\overline{\text{BO3}}$: $I_{OUT} = 2.0\text{ mA}$ | | | 1.0 | V |
| | V_{OL4} | P_{D1} , P_{D2} : $I_{OUT} = 0.1\text{ mA}$ | | | 0.3 | V |
| Output off leakage current | I_{OFF1} | $\overline{\text{SYC}}$: $V_{OUT} = 6.5\text{ V}$ | | | 5.0 | μA |
| | I_{OFF2} | $\overline{\text{BO1}}$ to $\overline{\text{BO3}}$: $V_{OUT} = 13\text{ V}$ | | | 3.0 | μA |
| Output high-level voltage | V_{OH} | P_{D1} , P_{D2} : $I_{OUT} = -0.1\text{ mA}$ | $0.5 V_{DD}$ | | | V |
| High-level 3-state off leakage current | I_{OFFH} | P_{D1} , P_{D2} : $V_{OUT} = V_{DD}$ | | 0.01 | 10.0 | nA |
| Low-level 3-state off leakage current | I_{OFFL} | P_{D1} , P_{D2} : $V_{OUT} = 0\text{ V}$ | | 0.01 | 10.0 | nA |
| Current drain | I_{DD1} | $V_{DD1} + V_{DD2}$: *2 | | 25 | 40 | mA |
| | I_{DD2} | V_{DD2} : PLL block stopped | | 2.0 | 3.5 | mA |
| Input capacitance | C_{IN} | FMIN | 1 | 2 | 3 | pF |

Note: 1. $V_{DD} = 3.5$ to 6.5 V

2. With a 7.2 MHz crystal connected between XIN and XOUT, $f_{IN2} = 130\text{ MHz}$, $V_{IN2} = 100\text{ mVrms}$, other input pins at V_{SS} , output pins open.

Oscillator Circuit Example



Kinseki, Ltd.

HC43/U: 2114-84521 (1): $CL = 10\text{ pF}$, $C1 = 15$ (10 to 22) pF , $C2 = 15\text{ pF}$

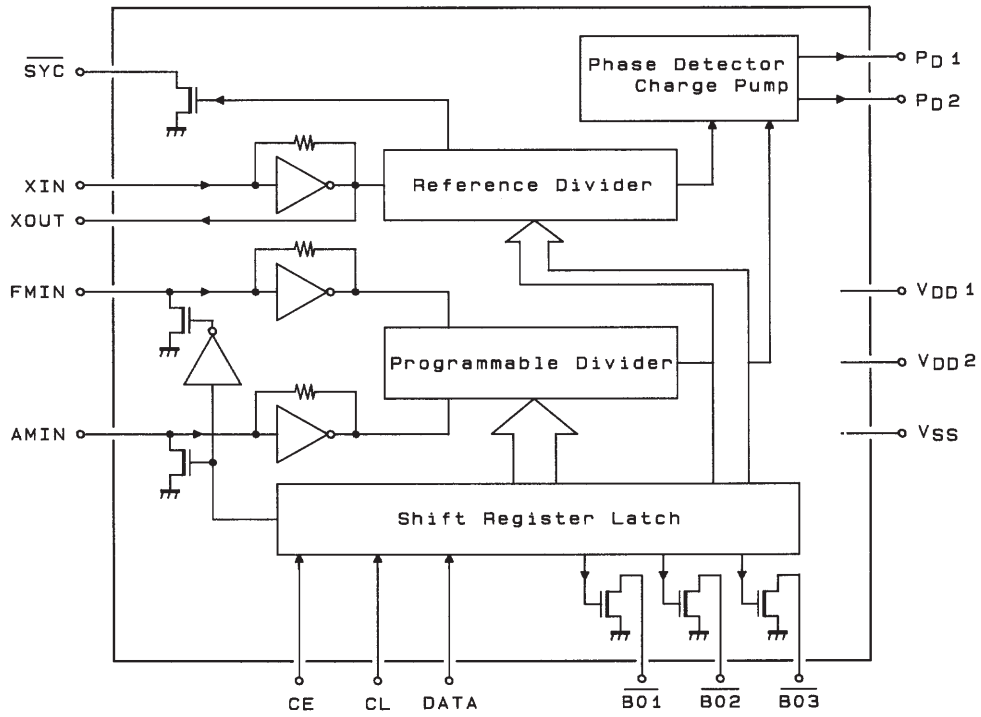
HC43/U: 2114-84521 (2): $CL = 16\text{ pF}$, $C1 = 22$ (15 to 33) pF , $C2 = 33\text{ pF}$

Nihon Denpa Kogyo, Ltd.

NR-18: LM-X-0701: $CL = 10\text{ pF}$, $C1 = 15\text{ pF}$, $C2 = 15\text{ pF}$

Since the circuit constants in the crystal oscillator circuit depend on the crystal element used and the printed circuit board pattern, we recommend consulting with the manufacturer of the crystal element concerning this circuit.

Equivalent Circuit Block Diagram



Pin Functions

| Symbol | Description |
|---|---|
| $\overline{\text{SYC}}$ | Controller clock (400 kHz) |
| XIN, XOUT | Crystal oscillator (7.2 MHz) |
| FMIN, AMIN | Local oscillator signal input |
| CE, CL, DATA | Data input |
| $\overline{\text{B01}}$ to $\overline{\text{B03}}$ | Band data output. $\overline{\text{B01}}$ can be used as a time base output (8 Hz). |
| V_{DD1} , V_{DD2} , V_{SS} | Power supply (Apply power to both V_{DD1} and V_{DD2} when the PLL circuit is operating. V_{DD2} is the crystal oscillator and time base power supply. Internal data cannot be maintained on V_{DD2} only.) |
| P_{D1} , P_{D2} | Charge pump output |

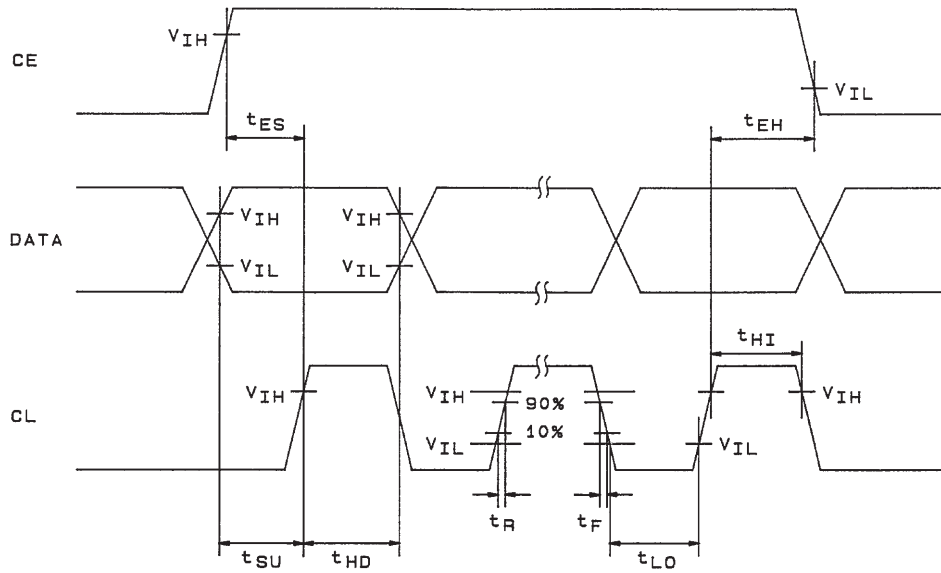
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Data Input Timing

$V_{IH} = 2.2$ to 6.5 V, $V_{IL} = 0$ to 0.7 V, $Xtal = 5.00$ to 7.20 (typ) to 8.00 MHz

Data acquisition: On the CL rising edge

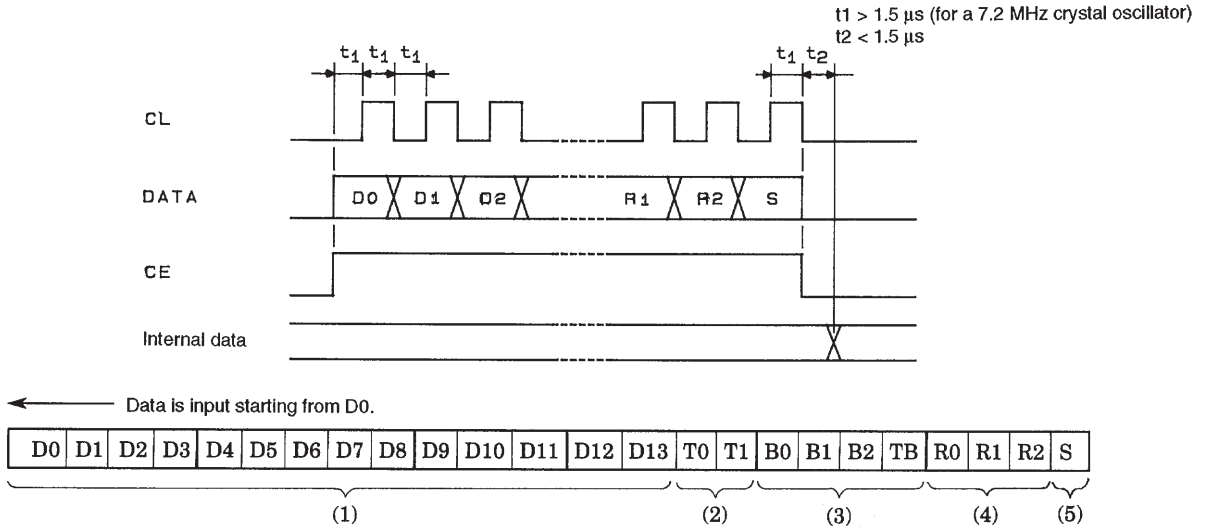
Note: Data transfers must be started only after the crystal oscillator is operating normally, i.e., after a proper input signal has been supplied to XIN.



A04896

| Parameter | Symbol | Xtal: 7.20 MHz | Xtal: for frequencies other than 7.2 MHz | Example: XIN = 2.048 MHz |
|-----------------------|----------|----------------------|---|--------------------------|
| Enable setup time | t_{ES} | At least 1.5 μ s | At least $\left[\frac{1 \times 8}{f_{Xtal}} \right] \times 1.35$ | At least 5.27 μ s |
| Enable hold time | t_{EH} | At least 1.5 μ s | At least $\left[\frac{1 \times 8}{f_{Xtal}} \right] \times 1.35$ | At least 5.27 μ s |
| Data setup time | t_{SU} | At least 1.5 μ s | At least $\left[\frac{1 \times 8}{f_{Xtal}} \right] \times 1.35$ | At least 5.27 μ s |
| Data hold time | t_{HD} | At least 1.5 μ s | At least $\left[\frac{1 \times 8}{f_{Xtal}} \right] \times 1.35$ | At least 5.27 μ s |
| Clock low-level time | t_{LO} | At least 1.5 μ s | At least $\left[\frac{1 \times 8}{f_{Xtal}} \right] \times 1.35$ | At least 5.27 μ s |
| Clock high-level time | t_{HI} | At least 1.5 μ s | At least $\left[\frac{1 \times 8}{f_{Xtal}} \right] \times 1.35$ | At least 5.27 μ s |
| Rise time | t_R | Up to 1 μ s | Up to 1 μ s | Up to 1 μ s |
| Fall time | t_F | Up to 1 μ s | Up to 1 μ s | Up to 1 μ s |

Data Input



- (1) D0 (LSB) to D13 (MSB): Divisor data
FMIN uses D0 to D13 and AMIN uses D4 to D13.

| | | | | | | | | | | | | | | | |
|-----|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----------------------------------|
| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | D12 | D13 | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | → | Example ①: FMIN divisor = 1007 |
| LSB | | | | | | | | | | | | | | MSB | |
| X | X | X | X | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | → | Example ②: AMIN divisor = 145 |
| LSB | | | | | | | | | | | | | | MSB | |

Sample calculation

- ① FM 100 kHz steps ($f_{ref} = 100 \text{ kHz}$)
FM VCO = 100.7 MHz (FM RF = 90.0 MHz, IF = 10.7 MHz)
Divisor = 100.7 MHz (FM VCO) ÷ 100 kHz (f_{ref}) = 1007 → 3EF_(HEX)
- ② AM 10 kHz steps ($f_{ref} = 10 \text{ kHz}$)
AM VCO = 1450 kHz (AM RF = 1000 kHz, IF = 450 kHz)
Divisor = 1450 kHz (AM VCO) ÷ 10 kHz (f_{ref}) = 145 → 91_(HEX)

- (2) T0 and T1 are LSI test bits and both should be set to 0.

- (3) B0 to B2, TB: Band data
Time base data

Note: *: Determined by R0 to R3. See item (4) on next page.

| Input | | | | Output | | |
|-------|----|----|----|--------|-----|-----|
| B0 | B1 | B2 | TB | BO1 | BO2 | BO3 |
| 0 | 0 | 0 | 0 | * | * | * |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | TB | * | * |
| X | 1 | 0 | 1 | TB | 1 | 0 |
| X | 0 | 1 | 1 | TB | 0 | 1 |
| X | 1 | 1 | 1 | TB | 1 | 1 |
| 1 | 0 | 0 | 1 | TB | 0 | 0 |

X: Don't care
TB: 8 Hz

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(4) R0 to R2: Reference frequency data

| R0 | R1 | R2 | f _{ref} [kHz] | $\overline{BO1}$ | $\overline{BO2}$ | $\overline{BO3}$ |
|----|----|----|------------------------|------------------|------------------|------------------|
| 0 | 0 | 0 | 100 | 1 | 1 | 0 |
| 0 | 0 | 1 | 50 | 1 | 1 | 0 |
| 0 | 1 | 0 | 25 | 1 | 1 | 0 |
| 0 | 1 | 1 | 5 | 0 | 0 | 1 |
| 1 | 0 | 0 | 10 | 1 | 0 | 1 |
| 1 | 0 | 1 | 9 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 5 | 0 | 0 | 1 |

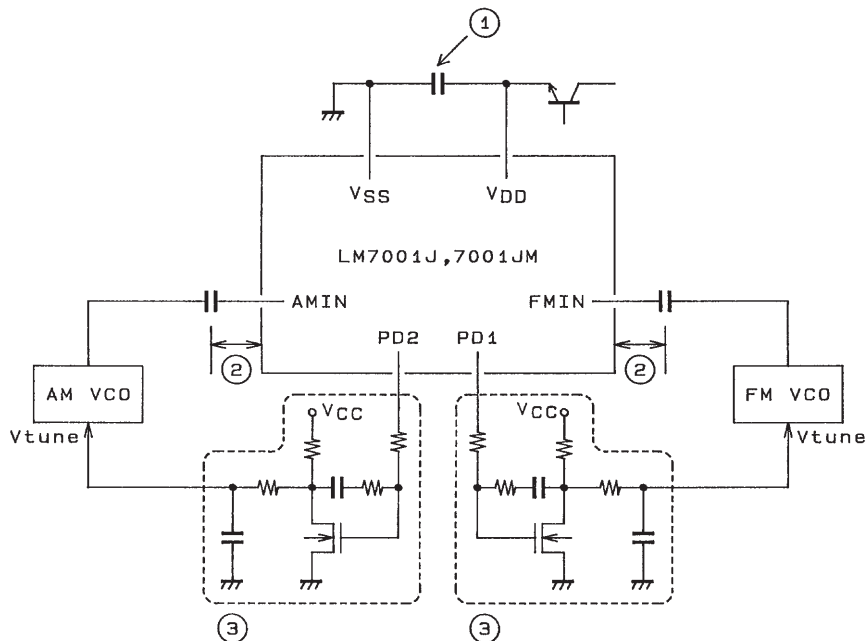
Note: The values listed for $\overline{BO1}$, $\overline{BO2}$, and $\overline{BO3}$ are for the case when the B0 to B2 data is set to all zeros.

(5) S: Divider selection data

1: FMIN, 0: AMIN

Notes on PLL IC Usage

1. PLL IC printed circuit board patterns



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① Power supply pins

A capacitor must be inserted between the V_{DD} and V_{SS} power supply pins for noise exclusion. This capacitor must be located as close as possible to these pins.

② FMIN and AMIN pins

The coupling capacitors must be located as close as possible to these pins.

③ PD pins, low-pass filter

Since these are high-impedance pins, they are susceptible to noise. Therefore, the pattern should be kept as short as possible and the area around this circuit should be covered by the ground pattern.

2. Initial states of the output ports ($\overline{BO1}$ to $\overline{BO3}$)

The initial states of the output ports after power is applied are undefined until data has been transferred.

In particular, it is possible for the $\overline{BO1}$ and $\overline{BO3}$ pins to output the internal clock, so data must be transferred as soon as possible.

However, note that the LSI cannot accept data until the crystal oscillator is operating normally.

3. VCO

The VCO circuit is designed so that it does not stop oscillating even if the control voltage (V_{tune}) becomes 0 V. (This is because the PLL circuit could become deadlocked if the VCO stopped.)

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